StackPC™ Specification

Version 1.2

July 14, 2014

Including Adoption on
PC/104, EBX, EPIC and 3.5” SBCs Form Factors

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REVISION HISTORY

Revision History is for this document. The initial draft Version 0.1 was written by Fastwel.

Dec 12, 2011 StackPC Specification draft Version 0.1 released by Fastwel for internal use only.

Feb 02, 2012 StackPC Specification draft Version 0.2 released by Fastwel for internal use only.

Changed 2.2 Pin Assignment, added Universal Types pin-outs for reference.

Changed section B.2.

Tables renumbered.

Added Figure 8-21.

Figures renumbered.

March 07, 2012 StackPC Specification draft Version 0.3 released by Fastwel for internal use only.

Changed sections 2.2 Pin Assignment, B.2.

Changed Figures 6-3, 6-4.

April 2, 2012 StackPC Specification Version 1.0 released by Fastwel.

Changed document structure.

Changed section B.2.

Tables renumbered.

Figures renumbered.

April 16, 2012 StackPC Specification Version 1.01 released by Fastwel.

Connector A pin 45 (DIR) description is clarified.

Changed Tables 2-1 (DIR added), 2-2 (STK0 resistor value, number of GND pins are changed).

Changed Tables 8-5, 8-6, 8-7 (DIR and Host ground pins added).

Changed Section 2.3 (more explanation on pass through and ground pins).

Changed Section B.3.5.

May 8, 2012 StackPC Specification Version 1.02 released by Fastwel.

One useless paragraph is removed from Section B.3.5

July 24, 2012 StackPC Specification Version 1.03 released by Fastwel.

Defined values and voltage level for STK[0:1] and Type_DETECT# pull-up resistors, section 2.3, page 27.

Defined values and voltage level for Config_Type[0:2] pull-up resistors, section 4.3, page 32.

Changed figure 8-26, page 61.

October 1, 2012 StackPC Specification Version 1.04 released by Fastwel.

Changed figure 8-26, page 61.

Added figure 8-27, page 62.

April 29, 2013 StackPC Specification Version 1.1 released by Fastwel.

Removed StackPC form-factor board outline dimensions.

Added StackPC connectors layout and dimensions.

July 14, 2014 StackPC Specification Version 1.2 released by Fastwel.

Defined FBUS signal assignment in Table 2-1 and Table 2-2.

Modified Figure 8-22: Reference schematic for StackPC modules with STK protection mechanism.

Added mounting holes on Figure 8-11.

Corrected FPE connector layout on Figure 8-30, Figure 8-32, Figure 8-34, Figure 8-37.

All pages are renumbered and font changed to Arial Unicode MS.

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GLOSSARY OF TERMS

Terms	Definitions
ATX	Advanced Technology Extended A specification for PC motherboards, power supplies, and system chassis. One of its most notable features is support for “Standby” and “Soft-Off” power savings modes.
StackPC	StackPC specifications. Refers also to boards containing only Basic “Expansion Connector A” (StackPC connector).
StackPC-PCI	Refers to boards containing Basic “Expansion Connector A” (StackPC connector) and “Expansion Connector B” with parallel PCI-bus (PCI-104 connector).
StackPC-FPE	Refers to boards containing Basic “Expansion Connector A” (StackPC connector) and “Expansion Connector B1” (FPE connector).
PCI-104	“Expansion Connector B” with parallel PCI bus. Refers also to PCI/104 form factor having mechanically and electrically compatible PCI bus connector.
FPE	"Fat Pipe Expansion" - optional high speed “Expansion Connector B1”.
Device	A logical device attached to a PCIe Link. Generally an add-in card.
EBX	Form factor for SBC’s
Host	The central connection of a PCIe system, typically a CPU module. This is called the “Root Complex” by the PCIe specification.
Lane	Fundamental unit of a PCI Express connection. A set of differential signal pairs, one pair for transmission, and one pair for reception. Multiple lanes may be combined to increase bandwidth (up to x16). A “by-N Link” is comprised of N Lanes.
Link	The collection of one or more PCI Express Lanes, plus an additional differential pair for a clock, which make up a standard PCI Express interconnect. According to PCI Express Specification 1.1 a Link can be comprised of 1, 4, 8, or 16 Lanes.
Packet Switch	A device used to attach multiple PCIe devices to a single link on the HOST. The PCIe Specification refers to this simply as a “Switch.” In this document, the term “Packet Switch” is used to differentiate from a “Signal Switch.”
PCIe	PCI Express
SBC	Single Board Computer
Signal Switch	An analog switch used to select between multiple PCIe devices to attach to a single PCIe link, or multiple links to attach to a single device. Also called a “Channel Switch.”

1. INTRODUCTION

1.1. Purpose

This document defines a new standard for stackable modular industrial computers based on modern serial interconnects for data exchange between modules such as PCI Express with x1, x4, x8 and x16 links, SATA, USB and Gigabit Ethernet. The standard gives an opportunity to use low bandwidth interconnects such as LPC, SPI and others for expansion of host computing boards with peripheral modules.

The purpose of this Specification is to provide a System level Stack-Up Only approach. Specification adopts PCI-Express, Ethernet, SATA, USB as well as LPC, SPI, Field Buses and Common Power Connector to the any stacked architecture.

StackPC Specification defines StackPC, FPE, StackPWR connectors relative position and stacked systems organization common approach. Also specification describes using stack modules in COM applications.

Specification is targeted not only for traditional stackable systems with all boards of the same form factor, but also for other stackable architectures like COM applications (mezzanine Computer-On-Module in conjunction with base board) and SBC expansion (expansion bus for Single Board Computers of various form factors).

PCI Express was chosen because of its performance, scalability and wide market acceptance.

Ethernet was chosen as the most popular long distance data interconnect, which is inevitable in modern computer based environments.

SATA was chosen as the storage interconnect because of wide acceptance and bandwidth scalability.

LPC bus, SPI and other signaling interfaces were chosen because of their capabilities to provide support for legacy devices and to expand host processor functionality in simple and cost effective way.

Additionally specification describes adoption StackPC to popular standards such as PC/104, 3.5 inch, EPIC and EBX. This adoption is as result of StackPC and PCIe/104 compatibility with Bank1 signals (same connector and similar pinout).

1.2. Standard Identification

This standard defines three versions of modules that are mechanically and electrically compatible with each other, but differ in a set of supported interfaces:

- StackPC. This version has one StackPC expansion connector. The following interfaces are supported:

4x1 PCIe	– 4 root ports, 4 clocks
1x4 PCIe	– 1 root port, 1 clock
USB 2.0	– 6 ports
SATA	– 2 ports
Gigabit Ethernet	– 2 ports
LPC	
FBUS	– 2 ports
SPI, SMB	

- StackPC-PCI. This version has two expansion connectors – StackPC and PCI-104. The following interfaces are supported:

4x1 PCIe	– 4 root ports, 4 clocks
1x4 PCIe	– 1 root port, 1 clock
PCI	– 32-bit, 33 MHz, support for up to four PCI-master devices
USB 2.0	– 6 ports
SATA	- 2 ports
Gigabit Ethernet	– 2 ports
LPC	
FBUS	– 2 ports
SPI, SMB	

- StackPC-FPE. This version has two expansion connectors – StackPC and FPE (Fat Pipe Expansion). The following interfaces are supported:

4x1 PCIe	– 4 root ports, 4 clocks
1x4 PCIe	– 1 root port, 1 clock
1x16/2x8/2x4 PCIe	– 2 root ports, 2 clocks
USB 2.0/3.0	– 6 ports
SATA	– 2 ports
Gigabit Ethernet	– 2 ports
Display Port	– 1 port
LPC	
FBUS	– 2 ports
SPI, SMB	
Configurable Section	

1.3. Description

StackPC specification is designed to deal with challenges caused by modern point-to-point high speed serial interfaces to stackable architecture which used to rely on traditional parallel bus interfaces. New specification is suitable for using for SBC expansion and fully opens Computer On Module like area of applications. It also paves the way for using even higher speed interfaces which are just emerging on embedded arena.

Compared to past years systems, modern embedded solutions require support for greater number of input/output interfaces. With each year, new processor modules support more and more input/output interfaces integrated in system logic. This makes necessary to place additional interface connectors on processor and peripheral modules. Compactness of Small Form Factor modules is an impediment to placement of necessary components and sufficient number of input/output connectors. It should be noted, that stackable modules are mostly designed for harsh environments and require installation inside an enclosure to protect them from mechanical impact or corrosive substances. Hence, embedded systems manufacturers have to resort to various tricks to bring out all interfaces to connectors on the front panel of enclosure using flat cables.

One of the solutions can be to aggregate the main set of input/output interfaces at the stack connectors. This allows to avoid some interface connectors (usually pin headers) and to provide more space on the module for placement of necessary components. This, in turn, leads to reduction of manufacturing cost and adds flexibility in terms of using the module in applications requiring limited functionality. Reducing cabling inside the enclosure improves convection, reduces magnetic noise pickup, and consequently, increases system effectiveness. Interfaces aggregated at the stack connectors can be led out of the enclosure using inexpensive and efficient solution – terminal interface module carrying the necessary set of standard interface connectors.

One of rather important requirements to the new specification is compatibility with family of PC/104 standards. The support for existing and field proven PC/104, PC/104-Plus, PCI/104, PCIe/104 and PCI/104-Express modules is provided. Details about compatibility between StackPC and PC/104 standards can be found in Appendix B.

StackPC specification defines following versions of modules:

1. StackPC. Only StackPC connector is mounted onboard to provide support for most popular high-speed and legacy interfaces. Four x1 and one x4 PCI Express links are supported simultaneously as well as USB 2.0 interfaces, Gigabit Ethernet, SATA and others. Modules in this form factor use basic set of interfaces which are required in most embedded applications.

2. StackPC-PCI. Two connectors are mounted onboard – StackPC and PCI-104. Modules in this form factor provide basic set of modern interfaces plus compatibility with still widely used modules having parallel PCI bus.

3. StackPC-FPE. In addition to basic StackPC connector an optional FPE (Fat Pipe Expansion) connector is used. This optional FPE connector brings extra 1x16 or 2x8 (x4, x1) PCI Express lanes, Display port and Configurable Section of signals in addition to basic set of StackPC interfaces. StackPC-FPE modules can be used for high performance and multimedia systems.

Figure 1-1 shows a basic view of StackPC layouts.

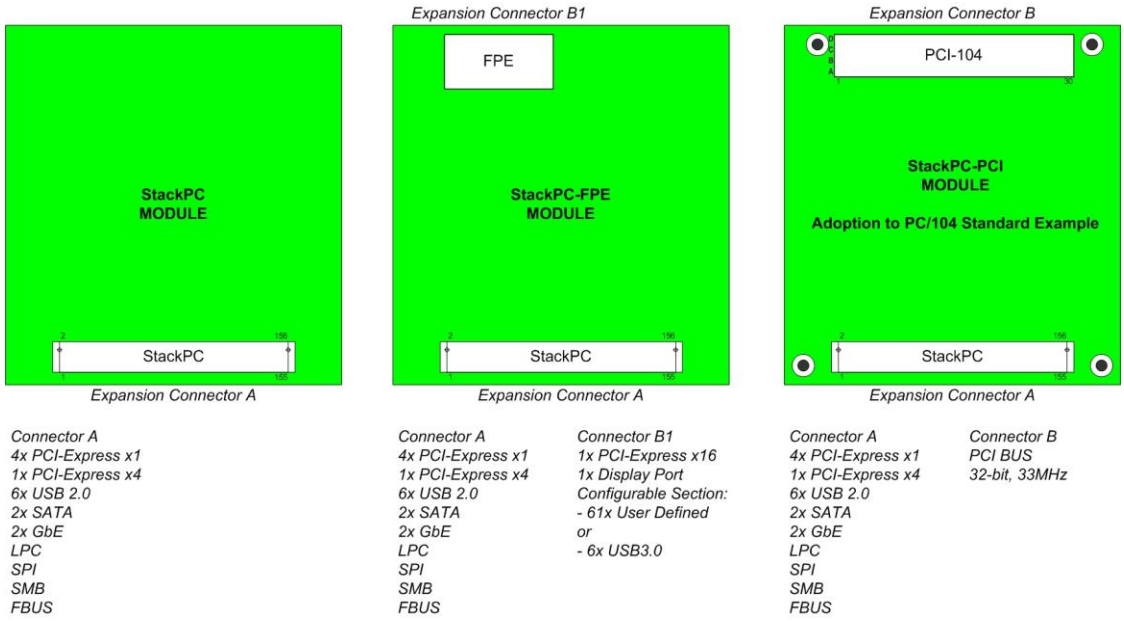


Figure 1-1: StackPC, StackPC-FPE and StackPC-PCI general board layouts

StackPC specification defines only one direction for modules stacking. Following that definition, StackPC peripheral modules are stacked on top side of Host board ("Stack-Up only" configuration). This allows Host module to be more functional and more cost efficient. Host module may be on top or bottom of system stack depending from the whole system stack orientation. CPU chip can be on top or bottom of Host module depending from chosen heat dissipation approach.

StackPC specification doesn't limit vendors on how they use Bottom side of Host module. To adopt StackPC module to PC/104 family standards additional PCIe-104 (Type 1 or Type 2) connector can be used on Bottom side providing Stack-Down configuration option or PCI-104 connector can be placed instead of FPE connector (see Figure 8-24). Depending on type of used PCIe-104 or PCI-104 connectors StackPC-PCI Host module may allow both Stack-Up and Stack-Down configurations for PCI/104 peripheral modules.

StackPC has following features:

Connector A:
4x1 PCIe – 4 root ports, 4 clocks
1x4 PCIe – 1 root port, 1 clock
USB 2.0 – 6 ports
SATA – 2 ports
Gigabit Ethernet – 2 ports
LPC
FBUS – 2 ports
SPI – 3 slaves
SMB
ATX power and control signals: +5V_SB, PS_ON#, POWERGOOD
Power: +3.3V, +5V, +12V

StackPC-PCI has the following features:

Connector A: The same as in StackPC
Connector B:
PCI Bus. Supports up to four 32 bit, 33 MHz PCI Bus cards each capable of Bus Mastering (same as on PC/104-Plus and PCI-104), +3.3V PCI signaling level
Power: +3.3V, +5V, +12V, -12V

StackPC-FPE has the following features:

Connector A: The same as in StackPC
Connector B1:
1x16 PCIe or 2x8 PCIe or 2x4 PCIe – 2 root ports, 2 clocks
Display Port – 1 port
Configurable Section - – User Defined
Power: +3.3V, +5V, +12V

1.4. Comparison to Other Standards

Table 1-1 presents comparison of different form factors by supported interfaces. Same color marks interfaces whose connectors are mechanically and electrically compatible, i.e. modules can be stacked without any intermediate adapter modules.

Table 1-1: Comparison of Different Form Factors

	ISA	PCI	x1 PCIe	x4 PCIe	x16 PCIe	USB 2.0	USB 3.0	SATA	GbE	LPC	SPI	SMB	User I/O	Other	Power
PC/104	1														+5V, -5V, +12V, -12V
PC/104-Plus	1	4 slots													+5V, -5V, +12V, -12V
PCI/104		4 slots													+3.3V, +5V, +5V_SB, +12V
PCIe/104 Type 1			4 root ports		1 x16 or 2 x8 or 2 x4 or 2 SDVO	2						1			+3.3V, +5V, +5V_SB, +12V
PCIe/104 Type 2			4 root ports	2 root ports		2	2	2		1		1			+3.3V, +5V, +5V_SB, +12V, RTC_Battery
PCI/104-Express		4 slots	4 root ports		1 x16 or 2 x8 or 2 x4 or 2 SDVO	2						1			+3.3V, +5V, +5V_SB, +12V, -12V
StackPC			4 root ports	1 root port		6		2	2	1	3	1		2x FBUS, 2 Express Cards	+3.3V, +5V, +5V_SB, +12V, RTC_Battery
StackPC-PCI		4 slots	4 root ports	1 root port		6		2	2	1	3	1		2x FBUS, 2 Express Cards	+3.3V, +5V, +5V_SB, +12V, -12V, RTC_Battery
StackPC-FPE			4 root ports	1 root port	1 x16 or 2 x8 or 2 x4	6		2	2	1	3	1	50	2x FBUS, 2 Express Cards, DisplayPort	+3.3V, +5V, +5V_SB, +12V, RTC_Battery
SUMIT A			1 root port			4				1	2	1		1 Express Card	+3.3V, +5V, +5V_SB, +12V
SUMIT B			1 root port	1 x4 or 2 x1											+3.3V, +5V, +5V_SB, +12V
Comit			3 root ports	1 x4 or 4 x1		6		2	1	1	2	1		VGA, LVDS, SDIO, Audio	+3.3V, +5V, +3.3V_SB, +5V_SB, RTC_Battery, +12V

The same color indicates that corresponding interfaces are directly mechanically and electrically compatible if different modules are in one stack.

1.5. StackPC typical applications

1.5.1 Stackable embedded computers.

Design of rugged miniature stackable computers is traditional area of using StackPC modules. StackPC allows building complete system as a stack of CPU and various peripheral modules. Power supply module also may have the same form factor and be a part of the same stack. StackPC also defines optional power connectors that allow system designers to deliver power to the stack with unified approach.

The whole StackPC stack may have individual enclosure or be a part of complex device having additional electronics for implementing human machine interface or other application specific functions.

Currently it is not usually easy task for system designer to have all necessary interfaces to be proper connected and wired. Since StackPC standardizes propagation of most popular interfaces through main stack connectors it significantly simplifies system wiring and give a new dimension for implementing system interconnects.

Figure 1-2 shows example of StackPC system in individual enclosure. Set of high speed interfaces are delivered to I/O connectors on interface module using standard high speed StackPC connector instead of wired connections.

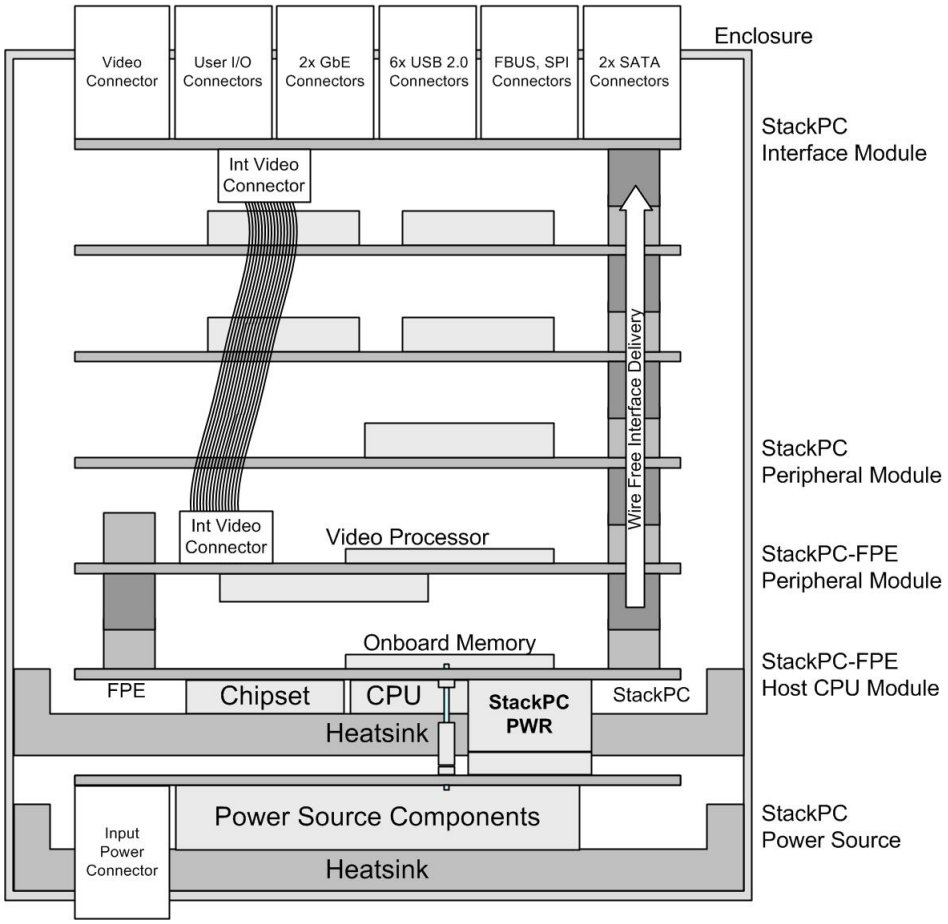


Figure 1-2: StackPC embedded system example

1.5.2 Expansion Bus for Single board Computers

StackPC specification can be adopted as an expansion connector for single board computers (SBCs) of various standards and customer specific form factors. This specification defines how to use StackPC as an expansion bus for EBX, EPIC and 3.5” alike single board computers. StackPC can also be used as an expansion bus for SBCs of other form factors until relative locations of StackPC connectors and mounting holes are met. Figure 1-3 shows example of using StackPC peripheral board together with EPIC single board computer.

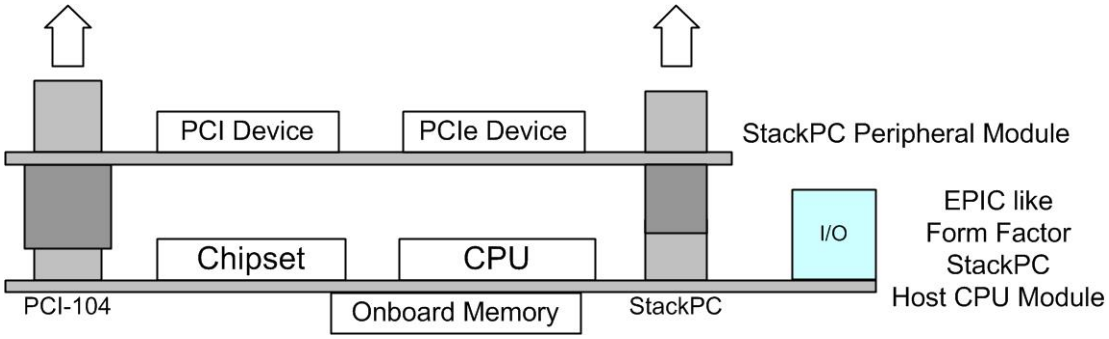


Figure 1-3: SBC expansion with StackPC peripheral module

For this kind of applications StackPC allows to expand SBC functionality with wide range of available peripheral modules. In addition to using standard PCIe lanes, StackPC peripheral modules can directly use SATA, USB 2.0, SPI, LPC, FBUS or Gigabit Ethernet interfaces available on Host SBC. It gives cost effective way of using SATA and USB storages, LPC, SPI, FBUS and Ethernet devices on peripheral modules without necessity to have PCI or PCIe interface chips or in system wiring.

1.5.3 Computer-On-Module for mounting on carrier board.

Having most popular peripheral interfaces within stack connectors StackPC opens the door to the new area of Computer-On-Module (COM) like applications which were not addressed by PC/104 family specifications. Figure 1-4 shows example of using StackPC-FPE CPU module as a Computer-On-Module mounted on application specific carrier board.

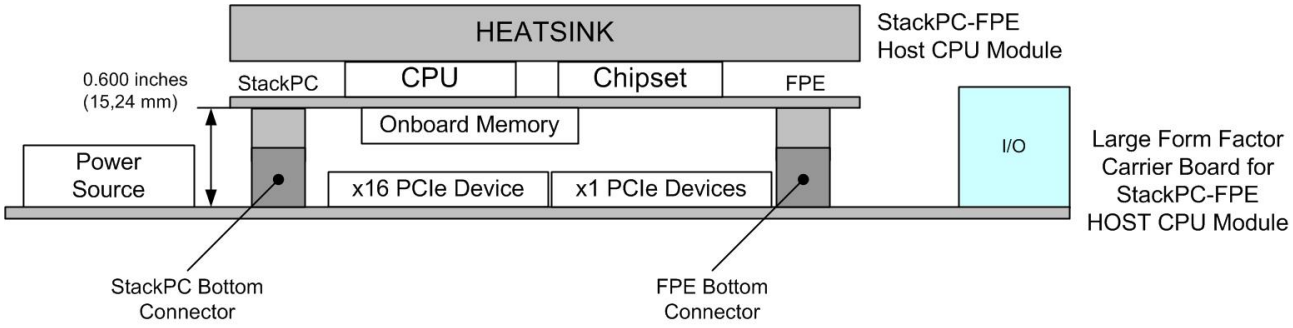


Figure 1-4: Computer-On-Module application of StackPC-FPE CPU module.

For many applications carrier board has rather tall peripheral connectors or there are no strict space limitations. In such cases it makes no sense to use low profile COM modules available on the market. Such low profile COM modules (like COM-express) put severe restrictions on height of components on COM modules and on carrier board within PCB area where COM module to be located. In practice

designers sometimes try to avoid placing any components in this area of carrier board. Using StackPC CPU module as a COM module does not apply such restrictions thus providing more flexibility and real estate for carrier board designers. Tall components can be used both on StackPC CPU module and on carrier board.

Additional unique feature of using StackPC CPU as a COM module is a possibility to add StackPC peripheral modules to the system. Figure 1-5 shows how system functionality can be extended by adding standard peripheral module between StackPC CPU and carrier board.

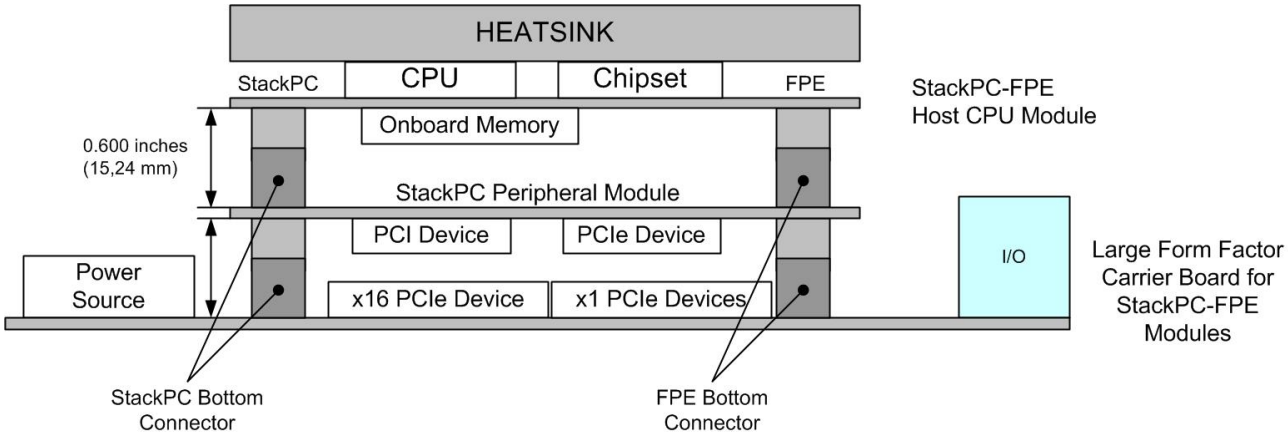


Figure 1-5: Computer-On-Module application of StackPC-FPE CPU and Peripheral modules stack.

1.6. StackPC signals groups descriptions

1.6.1 PCI Express Expansion Bus

Basic StackPC connector provides four x1 PCI Express links (required) and a single x4 PCI Express link (optional). Single x4 PCI Express link can be configured as four x1 links (optional).

Optional FPE connector adds extra 1x16 Link or 2x8 Links or 2x4 PCIe Links which can be used for applications where high I/O bandwidth and/or multimedia expansion are needed.

1.6.2 Express Card Interface

Low active PE_PRSNT[0:1]# signals indicate that one or two Express Cards with PCI Express interface are presented in System. These lines are pulled up on Host. For more details, please see Express Card specification.

1.6.3 PCI Expansion Bus

The PCI Expansion Bus is the same 32 bit, 33 MHz PCI bus found on the PC/104-plus and PCI-104 Specifications with the addition of +5V_SB, PSON#, and PME#.

1.6.4 System Clocking

The PCIe architecture is based on a 100 MHz reference clock. The Host may also employ spread spectrum clocking as defined in the PCI Express Base Specification to reduce EMI. In this case it is required that the Device uses the distributed clock as its reference clock. Using an on-board oscillator as a reference is not allowed.

StackPC does not define any termination on unused clock lines; therefore the Host is required to disable any unused clocks.

StackPC Host module provides four x1 and one x4 PCIe Links with separate clocks to support four x1 and one x4 PCIe Devices. StackPC-FPE has additional two clocks serving 1x16, 2x8 or 2x4 PCIe Links.

1.6.5 Universal Serial Bus

Universal Serial Bus (USB) is used to connect peripherals such as storage, media, pointing devices or any other devices to the host system. This interface provides path to get and to transfer data information from the peripherals to the host system with speed up to 480 Mbps for USB 2.0.

StackPC connector supports up to 6 USB 2.0 ports. Line shifting is applicable to all USB ports as one group.

Host board provides only differential lines to the StackPC connector. Power for USB devices, should be provided by peripheral module to which they are connected.

The USB_OC# signal is used by peripheral modules to indicate Over Current event to the Host. Any USB port in case of Over Current situation should pull low the USB_OC# signal.

For more information, please refer to Universal Serial Bus Specifications.

1.6.6 Serial ATA Interface

Serial ATA (SATA) interface is used to connect storage peripherals such as hard drives, solid state drives, optical drives, etc. and to the host system. This interface is an evolutionary replacement for the Parallel ATA physical storage interface. StackPC connector supports 2 SATA ports with link shifting.

For more information, please refer to SATA Specification.

1.6.7 Gigabit Ethernet

StackPC specification defines group of two Gigabit Ethernet (GbE) ports without galvanic isolation, i.e. peripheral modules, having I/O connectors for these ports should include all necessary components for implementing physical layer, galvanic isolation, Power-Over-Ethernet, etc. Link shifting is applicable.

1.6.8 Low Pin Count Interface

This interface is used for legacy I/O devices support and may be considered as ISA bus replacement for peripheral devices such as Super I/O or user FPGA. LPC interface supports I/O, Memory, DMA and Bus Master cycles while its data transfer rate is higher than ISA bus. LPC interface supports 4GB memory space.

For more information, please refer to LPC Specification.

1.6.9 Field Bus Interface

Two FBUS ports can be considered as a User defined serial interfaces. It is 3.3V CMOS level serial interfaces which can be driven by UART, CAN controller, or by custom logic implementing user defined protocol. Converting CMOS levels to interface signals according particular physical layer requirements (RS-232, RS-422/485, CAN, etc), is the function of peripheral module. Peripheral modules can provide also galvanic isolation in case it is necessary. FBUS ports may be driven by Host or by Peripheral modules. In case FBUS is driven by Peripheral module this module should connect FBUS lines to Top connector only.

Each port has Rx, Tx or Positive, Negative lines and RTS# lines. Link shifting is applicable.

1.6.10 Serial Peripheral Interface

The optional Serial Peripheral Interface is a four-wire interface with separate Slave Select (SS#) signal to address peripheral device. This specification defines three SS# signals to support up to three peripheral devices without any address decoding on peripheral modules.

The SPI supports Master, Slave and Bi-directional modes for communication with peripheral devices. For more information, please see SPI Block Guide from Freescale Semiconductor (see Table 1-2). SS# signals link shifting is applicable.

1.6.11 System Management Bus

The optional System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I2C. SMBus provides a control bus for system and power management related tasks. A system may use SMBus to pass messages to and from devices instead of using individual control lines. Removing the individual control lines reduces pin count. Accepting messages ensures future expandability. With SMBus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspended event, report different types of errors, accept control parameters, and return its status. SMBus is described in System Management Bus (SMBus) Specification, Version 2.0. Refer to this specification for DC characteristics and all AC timings. If the system board or add-in card supports SMBus, it must adhere to additional requirements that can be found in Chapter 8 of the PCI Local Bus Specification, Revision. 3.0.

SMBus 2.0 Specification defines an address Resolution Protocol (ARP) that is used to assign slave addresses to SMBus devices. Although optional in the SMBus 2.0 Specification, it is required that systems that connect the SMBus to PCI slots implement ARP for assignment of SMBus slave addresses to SMBus interface devices on PCI add-in cards. The system must execute ARP on a logical SMBus whenever any PCI bus segment associated with the logical SMBus exits the B3 state or a device in an individual slot associated with the logical SMBus exits the D3 cold state. Prior to executing ARP, the system must ensure that all ARP-capable SMBus interface devices are returned to their default address state.

The system board provides pull-ups to the +3.3Vaux rail per the above specification and the components attached to these signals need to have a 3.3V signaling tolerance (5V signaling must not be used). Also, the SMBus is used during all power states, so all components attached to the SMBus must remain powered during standby, or ensure that the bus is not pulled down when not powered.

The SMBus interface is based upon the System Management Bus Specification (SMBus 2.0 Specification). This two-wire serial interface has low power and low software overhead characteristics that make it well suited for low-bandwidth system management functions.

The capabilities enabled by the SMBus interface include, but are not limited to, the following:

Support for client management technologies.
Support for server management technologies.
Support for thermal sensors and other instrumentation devices on StackPC modules.
Peripheral modules identification when the bus is in the B3 state or when the PCI device is in the D3hot or D3cold states as defined in the PCI Power Management Interface Specification.

1.6.12 Stack Control Signals

Stack control signals allow StackPC and PCIe/104 modules to define type and set of interfaces used by other modules in the same stack. That information is used to protect modules from being damaged if modules with conflicting interfaces are mixed in one stack. Detailed information on Stack Control Signals and rules can be found in Appendix B.

1.6.12.1 Type_DETECT# Signal

This signal is pulled up on StackPC Host. StackPC peripherals pass through this signal. PCIe/104 peripherals drive this signal to Low Level in case peripheral module uses interfaces which may cause conflict with StackPC specific interfaces.

1.6.12.2 STK0, STK1, STK2 Signals

These signals are used for detecting interfaces conflicts between modules of different types in case they are mixed in one stack. PCIe/104 modules generate Bus Stacking Error event depending on status of STK0…2 signals. StackPC modules generate Bus Stacking Error event depending on status of STK0…2 and Type_DETECT# signals.

1.6.12.3 Stack Direction (DIR) Signal

DIR signal is defined in PCIe/104 specification. Since StackPC specification defines only Stack-Up configuration with peripheral modules stacked only on Top of Host module, then StackPC Host module puts GND to pin 45 of Expansion A connector. Peripheral modules should pass through this signal. StackPC peripheral modules can work only on TOP of the PCIe/104 HOST module.

StackPC peripheral modules may use DIR signal to detect wrong stacking configuration. High Level on DIR signal can be used to indicate to end user that StackPC module is mistakenly stacked down.

1.6.13 ATX and Power Management

StackPC incorporates all necessary control and signal lines for ATX and power management functions. These signals include PWRGOOD, PSON#, +5V_SB, and PME#. The inclusion of these signals allows maximum power saving. All these signals are optional and all modules in one stack should work properly even if ATX and power management is not implemented.

1.6.13.1 Power Good (PWRGOOD) Signal

PWRGOOD is a “power good” signal. It should be asserted high by the power supply to indicate that the +12 VDC, +5 VDC, and +3.3 VDC outputs are above the under-voltage thresholds and that sufficient main energy is stored by the converter to guarantee continuous power operation within specifications. Conversely, PWRGOOD should be de-asserted to a low state when any of the +12 VDC, +5 VDC, or +3.3 VDC output voltages falls below its under-voltage threshold, or when main-power has been removed for a sufficiently long enough time that the power supply operation cannot be guaranteed beyond the power-down warning time. If Powergood is not supported then all modules in stack should start with its own internal control.

1.6.13.2 Power Supply On (PSON#) Signal

PSON# is an active-low signal that allows a CPU module to remotely control the power supply in conjunction with features such as soft on/off, Wake-on-LAN, or wake-on-modem. It is pulled up to +5V_SB line. When PSON# is driven to Low Level, the power supply should turn on the main DC output rails: +12 VDC, +5 VDC, +3.3 VDC, -12 VDC. When PSON# is pulled to High Level or open-circuited, the DC output rails should not deliver current and should be held at zero potential with respect to ground. PSON# has no effect on the +5V_SB output, which is always enabled whenever AC power is present.

CPU module should not drive PSON# signal Low in case Bus Stacking Error detected. PSON# signal can be used for indication that interface conflict has happened in stack.

1.6.13.3 +5V StandBy (+5V_SB)

+5V_SB is a standby supply output that is active whenever AC power is present. It provides a power source for circuits that must remain operational when the main DC output rails are in a disabled state. Example uses include soft power control, Wake-on-LAN, wake-on-modem, intrusion detection, or suspend state activities.

+5V_SB power is used to obtain +3.3V_SB power to support PME# or WAKE# functionality.

1.6.13.4 Power Management Event (PME#) Signal

The PME# signal is an active-low, open-drain signal that can be used by a device to request a change in the device or system power state. This signal can be shared among all devices in the system. Devices must be enabled by software before asserting this signal. Once asserted, the device must continue to drive the signal low until software explicitly clears the condition in the device.

The use of PME# is specified in the PCI Bus Power Management Interface Specification. Host and Devices using PME# must pull-up it to +3.3V_SB. Modules that do not use PME# signal have associated pin unconnected.

When the man power is turned off modules supporting PME# use +5V_SB power for generating power management events.

1.6.13.5 WAKE# Signal

The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express function to reactivate the PCI Express Link hierarchy's main power rails and reference clocks. Only modules that support the wake process connect to this pin. If the module has wake capabilities, it must support the WAKE# function. Likewise, only systems that support the WAKE# function need to connect to this pin, but if they do, they must fully support the WAKE# function. If the wake process is used, the +3.3V_SB supply must be present and used for this function. The assertion and de-assertion of WAKE# are asynchronous to any system clock.

If the WAKE# signal is supported, the signal is sent to the system's power management (PM) controller. Host and Device modules must provide a pull-up to +3.3V_SB on this signal, if they are allows the signal to be used. Boards that do not use this signal are not required to drive this signal or provide pull-ups on it.

WAKE# is not PME# and should not be attached to the PCI-PME# interrupt signals. WAKE# causes power to be restored but must not directly cause an interrupt.

According to PCIe/104 specification, systems using Type 2 peripheral modules do not support WAKE# signal. For compatibility reasons some StackPC modules do not support WAKE# signal as well. Section B.3.5 describes how to get WAKE# signal always available in StackPC systems.

1.6.13.6 RTC Battery

RTC_Battery pin allows optional battery power for StackPC modules.

Battery cell can be placed on any module in the stack with its own resistor and diode as shown on Figure 1-6.

Battery power can be used by any module (consumer) in the stack. For longer battery life it is recommended that total battery current is less than 5 uA. RC-filter for each consumer is required.

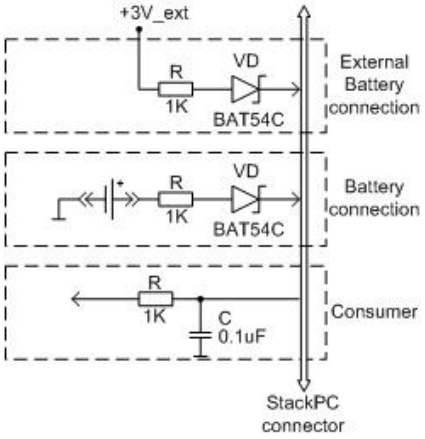


Figure 1-6: Example of using Battery power in StackPC stack.

1.7. References

The following documents should be used as reference for a detailed understanding of the overall system requirements. For latest revisions of the above specifications contact the respective organizations.

Table 1-2: References

ATX Specification Version 2.2	**Intel Corporation**	www.intel.com
Low Pin Count Interface Specification Revision 1.1	**Intel Corporation**	www.intel.com
PC/104 Specification Version 2.5	**PC/104 Embedded Consortium**	www.pc104.org
PC/104-*Plus* Specification Version 2.0	**PC/104 Embedded Consortium**	www.pc104.org
PCI-104 Specification Version 1.0	**PC/104 Embedded Consortium**	www.pc104.org
PCIe/104 & PCI/104-Express Specification Version 2.0	**PC/104 Embedded Consortium**	www.pc104.org
PCI Local Bus Specification Revision 2.2	**PCI Special Interest Group**	www.pcisig.com
PCI Express Base Specification Revision 1.1	**PCI Special Interest Group**	www.pcisig.com
ExpressCard Standard Release 2.0	**USB Implementers Forum**	www.usb.org
Serial ATA Revision 3.0 Specification	**SATA International Organization**	www.sata-io.org
Serial Peripheral Interface (SPIV3) Block Description V3.06	**Freescale Semiconductor**	www.freescale.com
System Management Bus (SMBus) Specification Version 2.0	**SBS Implementers Forum**	www.sbs-forum.org
Universal Serial Bus (USB 2.0) Specification Revision 2.0	**USB Implementers Forum**	www.usb.org
Universal Serial Bus 3.0 (USB 3.0) Specification Revision 1.0	**USB Implementers Forum**	www.usb.org
Ethernet IEEE 802.3 Standard	**IEEE Standards Association**	standards.ieee.org

If errors are found in this document, please send a written copy of the suggested corrections to the publishers listed on the title page.

1.8. Signal Naming Convention

Signals on StackPC and FPE connectors are named so that signal groupings are obvious. The fields in a signal name go from general to specific.

The PCI Express signals start with the characters “PE,” followed by the width of the Link (“x1”, “x4”), followed by an underscore “_”. Next is the Link number if there is more than one Link of that width. Then there is either “T”, “R”, or “CLK” for Transmit, Receive, or Clock respectively. Next is the lane number in the link in parenthesis, for the links that have more than one lane. The last symbol is “p” or “n” for the

positive and negative signal in the differential pair. For example, PEx4_0T(2)p is the positive signal in lane number 2 of the first x4 Link.

A signal on the connector is designated “transmit” or “receive” in a Host-centric manner. The “transmit” pin on the Host connects to the “T” (transmit) pin of the connector. From there, the signal connects to “receive” pin of the Device.

In a PCIe system the transmit pins of the chip are always connected to the receive pins of the other chip in the link, and vice-versa. For example, for a specific link, transmit on the Host chip is connected to receive on the Device chip, and receive on the Host is connected to transmit on the Device.

Other non-PCIe signals (SATA, LPC, SPI, FBUS, Display port) follow a similar convention.

2. EXPANSION CONNECTOR A (StackPC)

Expansion Connector A is the main connector containing basic set of modern interfaces. It is self-sufficient and can be the only connector in most embedded designs with StackPC architecture.

2.1. Functions

- Four x1 PCIe
- One x4 PCIe
- Six USB 2.0
- Two SATA
- Two Gigabit Ethernet
- LPC
- SPI with three Slave Select lines
- SMB
- Two FBUS
- ATX power and control signals: +5V_SB, PS_ON#, POWERGOOD
- Power: +3.3V, +5V, +12V, RTC_Battery

Since not all chipsets support all defined interfaces, it is up to the Host vendor to determine the type and number of implemented interfaces. However, implemented interfaces must comply with the pin out described below for Expansion Connector A. This will ensure that any peripheral module with, for example x1 PCI-Express Links will work with any Host that supports x1 PCI-Express Links.

2.2. Pin Assignment

StackPC connector has odd numbered pins located towards the edge of the board while even numbered pins are located towards the center of the board. Pin assignment is defined in Table 2-1.

Top View of Signal Assignment for StackPC connector for **Host & Peripheral** boards is shown on the left Column in Table 2-1.

Bottom View of Signal Assignment for StackPC connector for **Peripheral** boards is shown on the right Column in Table 2-1.

Note: StackPC connector is allowed only on Top of Host modules thus providing support for stacking StackPC peripheral modules only on Top of Host module.

Table 2-1: StackPC Connector A Pin Assignments

StackPC Assignment, Top View (Connector A)							StackPC Assignment, Bottom View (Connector A)						
	1	USB_OC#		PE_RST#	2			2	PE_RST#		USB_OC#	1	
	3	3.3V		3.3V	4			4	3.3V		3.3V	3	
	5	USB_1p		USB_0p	6			6	USB_0p		USB_1p	5	
	7	USB_1n		USB_0n	8			8	USB_0n		USB_1n	7	
	9	GND		GND	10			10	GND		GND	9	
	11	PEx1_1Tp		PEx1_0Tp	12			12	PEx1_0Tp		PEx1_1Tp	11	
	13	PEx1_1Tn		PEx1_0Tn	14			14	PEx1_0Tn		PEx1_1Tn	13	
	15	GND		GND	16			16	GND		GND	15	
	17	PEx1_2Tp		PEx1_3Tp	18			18	PEx1_3Tp		PEx1_2Tp	17	
	19	PEx1_2Tn		PEx1_3Tn	20			20	PEx1_3Tn		PEx1_2Tn	19	
	21	GND		GND	22			22	GND		GND	21	
	23	PEx1_1Rp		PEx1_0Rp	24			24	PEx1_0Rp		PEx1_1Rp	23	
	25	PEx1_1Rn	+5 Volts	PEx1_0Rn	26		BANK 1	26	PEx1_0Rn	+5 Volts	PEx1_1Rn	25	
	27	GND		GND	28			28	GND		GND	27	
	29	PEx1_2Rp		PEx1_3Rp	30			30	PEx1_3Rp		PEx1_2Rp	29	
	31	PEx1_2Rn		PEx1_3Rn	32			32	PEx1_3Rn		PEx1_2Rn	31	
	33	GND		GND	34			34	GND		GND	33	
	35	PEx1_1Clkp		PEx1_0Clkp	36			36	PEx1_0Clkp		PEx1_1Clkp	35	
	37	PEx1_1Clkn		PEx1_0Clkn	38			38	PEx1_0Clkn		PEx1_1Clkn	37	
	39	+5V_SB		+5V_SB	40			40	+5V_SB		+5V_SB	39	
	41	PEx1_2Clkp		PEx1_3Clkp	42			42	PEx1_3Clkp		PEx1_2Clkp	41	
	43	PEx1_2Clkn		PEx1_3Clkn	44			44	PEx1_3Clkn		PEx1_2Clkn	43	
	45	GND (DIR)		PWRGOOD	46			46	PWRGOOD		GND (DIR)	45	
	47	SMB_DAT		PE_x4_CLKp	48			48	PE_x4_CLKp		SMB_DAT	47	
	49	SMB_CLK		PE_x4_CLKn	50			50	PE_x4_CLKn		SMB_CLK	49	
	51	SMB_ALERT#		PSON#	52			52	PSON#		SMB_ALERT#	51	
Toward edge of board	53	STK0 / WAKE#		STK1 / SATA_ACT#	54	Toward center of board		54	STK1 / SATA_ACT#		STK0 / WAKE#	53	Toward edge of board
	55	Type_DETECT#		GND	56			56	GND		Type_DETECT#	55	
	57	ETH_0_MDI(0)p		PEx4_0T(0)p	58			58	PEx4_0T(0)p		ETH_0_MDI(0)p	57	
	59	ETH_0_MDI(0)n		PEx4_0T(0)n	60			60	PEx4_0T(0)n		ETH_0_MDI(0)n	59	
	61	GND		GND	62			62	GND		GND	61	
	63	ETH_1_MDI(0)p		PEx4_0T(1)p	64			64	PEx4_0T(1)p		ETH_1_MDI(0)p	63	
	65	ETH_1_MDI(0)n		PEx4_0T(1)n	66			66	PEx4_0T(1)n		ETH_1_MDI(0)n	65	
	67	GND		GND	68			68	GND		GND	67	
	69	ETH_0_MDI(1)p		PEx4_0T(2)p	70			70	PEx4_0T(2)p		ETH_0_MDI(1)p	69	
	71	ETH_0_MDI(1)n		PEx4_0T(2)n	72			72	PEx4_0T(2)n		ETH_0_MDI(1)n	71	
	73	GND		GND	74			74	GND		GND	73	
	75	ETH_1_MDI(1)p		PEx4_0T(3)p	76			76	PEx4_0T(3)p		ETH_1_MDI(1)p	75	
	77	ETH_1_MDI(1)n		PEx4_0T(3)n	78			78	PEx4_0T(3)n		ETH_1_MDI(1)n	77	
	79	ETH_1_LINK_ACT#	+5 Volts	ETH_0_LINK_ACT#	80		BANK 2	80	ETH_0_LINK_ACT#	+5 Volts	ETH_1_LINK_ACT#	79	
	81	SATA_T1p		SATA_T0p	82			82	SATA_T0p		SATA_T1p	81	
	83	SATA_T1n		SATA_T0n	84			84	SATA_T0n		SATA_T1n	83	
	85	GND		GND	86			86	GND		GND	85	
	87	USB_3p		USB_2p	88			88	USB_2p		USB_3p	87	
	89	USB_3n		USB_2n	90			90	USB_2n		USB_3n	89	
	91	GND		GND	92			92	GND		GND	91	
	93	USB_5p		USB_4p	94			94	USB_4p		USB_5p	93	
	95	USB_5n		USB_4n	96			96	USB_4n		USB_5n	95	
	97	GND		GND	98			98	GND		GND	97	
	99	ETH_1_CTREF		ETH_0_CTREF	100			100	ETH_0_CTREF		ETH_1_CTREF	99	
	101	SPI_MOSI		SPI_SS0#	102			102	SPI_SS0#		SPI_MOSI	101	
	103	SPI_MISO		SPI_SS1#	104			104	SPI_SS1#		SPI_MISO	103	
	105	STK2 / SPI_SCK		LPC_CLK	106			106	LPC_CLK		STK2 / SPI_SCK	105	
	107	SPI_SS2#		GND	108			108	GND		SPI_SS2#	107	
	109	ETH_0_MDI(2)p		PEx4_0R(0)p	110			110	PEx4_0R(0)p		ETH_0_MDI(2)p	109	
	111	ETH_0_MDI(2)n		PEx4_0R(0)n	112			112	PEx4_0R(0)n		ETH_0_MDI(2)n	111	
	113	GND		GND	114			114	GND		GND	113	
	115	ETH_1_MDI(2)p		PEx4_0R(1)p	116			116	PEx4_0R(1)p		ETH_1_MDI(2)p	115	
	117	ETH_1_MDI(2)n		PEx4_0R(1)n	118			118	PEx4_0R(1)n		ETH_1_MDI(2)n	117	
	119	GND		GND	120			120	GND		GND	119	
	121	ETH_0_MDI(3)p		PEx4_0R(2)p	122			122	PEx4_0R(2)p		ETH_0_MDI(3)p	121	
	123	ETH_0_MDI(3)n		PEx4_0R(2)n	124			124	PEx4_0R(2)n		ETH_0_MDI(3)n	123	
	125	GND		GND	126			126	GND		GND	125	
	127	ETH_1_MDI(3)p		PEx4_0R(3)p	128			128	PEx4_0R(3)p		ETH_1_MDI(3)p	127	
	129	ETH_1_MDI(3)n		PEx4_0R(3)n	130			130	PEx4_0R(3)n		ETH_1_MDI(3)n	129	
	131	PE_PRSNT1#	+12 Volts	PE_PRSNT0#	132		BANK 3	132	PE_PRSNT0#	+12 Volts	PE_PRSNT1#	131	
	133	SATA_R1p		SATA_R0p	134			134	SATA_R0p		SATA_R1p	133	
	135	SATA_R1n		SATA_R0n	136			136	SATA_R0n		SATA_R1n	135	
	137	GND		GND	138			138	GND		GND	137	
	139	FBUS_1TX(p)		FBUS_0TX(p)	140			140	FBUS_0TX(p)		FBUS_1TX(p)	139	
	141	FBUS_1RX(n)		FBUS_0RX(n)	142			142	FBUS_0RX(n)		FBUS_1RX(n)	141	
	143	GND		GND	144			144	GND		GND	143	
	145	LPC_AD0		LPC_DRQ#	146			146	LPC_DRQ#		LPC_AD0	145	
	147	LPC_AD1		LPC_SERIRQ#	148			148	LPC_SERIRQ#		LPC_AD1	147	
	149	GND		GND	150			150	GND		GND	149	
	151	LPC_AD2		LPC_FRAME#	152			152	LPC_FRAME#		LPC_AD2	151	
	153	LPC_AD3		*RTC_Battery*	154			154	*RTC_Battery*		LPC_AD3	153	
	155	FBUS_1RTS#		FBUS_0RTS#	156			156	FBUS_0RTS#		FBUS_1RTS#	155	

USB Interface
PCI-Express Interface
ATX Power Supply
SMBus Interface
SPI Bus
Field Bus Interface
LPC Bus
SATA Interface
Ethernet Interface
Power Interface
Type DETECT pin

2.3. Signal Descriptions

Table 2-2: Connector A (StackPC) Signals

Group	Pins	Signal Name	Host Direction	Description
x1 PCIe Links	4	PEx1_[0:3]Tp	Output	**Transmit Differential Upper Line** for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Tn	Output	**Transmit Differential Lower Line** for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Rp	Input	**Receive Differential Upper Line** for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]Rn	Input	**Receive Differential Lower Line** for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]CLKp	Output	**Clock Differential Upper Line** for x1 Links 0, 1, 2, 3. Shifted when used.
	4	PEx1_[0:3]CLKn	Output	**Clock Differential Lower Line** for x1 Links 0, 1, 2, 3. Shifted when used.
x4 PCIe Links	4	PEx4_0T(0:4)p	Output	**Transmit Differential Upper Lines** for the x4 Link.
	4	PEx4_0T(0:4)n	Output	**Transmit Differential Lower Lines** for the x4 Link.
	4	PEx4_0R(0:4)p	Input	**Receive Differential Upper Lines** for the x4 Link.
	4	PEx4_0R(0:4)n	Input	**Receive Differential Lower Lines** for the x4 Link.
	1	PEx4_0CLKp	Output	**Clock Differential Upper Line** for the x4 Link.
	1	PEx4_0CLKn	Output	**Clock Differential Lower Line** for the x4 Link.
PCIe	1	PE_RST#	Output	**Reset** for PCI Express Bus
	1	PE_PRSNT[0:1]#	Input	**PRESENT** signal for Express Cards. Shifted when used.
	1	STK0/WAKE#	Input	**Wake on Lan** signal for HOST module. Open Drain on peripheral modules
SATA	1	STK1/SATA_ACT#	Output	**SATA or IDE Activity Indication.** For External LED connection.
	2	SATA_[0:1]Tp	Output	**Transmit Differential Upper Line** for SATA interfaces.
	2	SATA_[0:1]Tn	Output	**Transmit Differential Lower Line** for SATA interfaces.
	2	SATA_[0:1]Rp	Input	**Receive Differential Upper Line** for SATA interfaces.
	2	SATA_[0:1]Rn	Input	**Receive Differential Lower Line** for SATA interfaces.
Gigabit Ethernet	8	ETH_[0:1]_MDI(0:3)p	Bidirectional	**Differential Upper Line** for Gigabit Ethernet.
	8	ETH_[0:1]_MDI(0:3)n	Bidirectional	**Differential Lower Line** for Gigabit Ethernet.
	2	ETH_[0:1]_LINK_ACT#	Output	**Link Activity Indication.** Shifted when used.
	2	ETH_[0:1]_CTREF		**Central line for Magnetic Transformers.** Shifted when used.
SMB	1	SMB_Clk	Output	**Clock** for SMBus
	1	SMB_Data	Bidirectional	**Data** for SMBus
	1	SMB_Alert#	Input	**Alert** for SMBus
SPI	1	SPI_MOSI	Output	**Master Out/Slave In** for SPI interface
	1	SPI_MISO	Input	**Master In/Slave Out** for SPI interface
	1	STK2/SPI_SCK	Output	**Serial Clock** for SPI interface.
	3	SPI_SS[0:2]#	Output	**Slave Select** for SPI interface. Shifted when used.
LPC	4	LPC_AD[0:3]	Bidirectional	**Multiplexed Command, Address, and Data** for LPC interface
	1	LPC_DRQ#	Input	**Encoded DMA/Bus Master Request** for LPC interface
	1	LPC_FRAME#	Output	**Frame** for LPC interface
	1	LPC_SERIRQ#	Input	**Serialized IRQ** for LPC interface
	1	LPC_CLK	Output	**Clock** for LPC interface
USB	6	USB_[0:5]p	Bidirectional	**Data Differential Upper Line** for the USB 2.0 interfaces.
	6	USB_[0:5]n	Bidirectional	**Data Differential Lower Line** for the USB 2.0 interfaces.
	1	USB_OC#	Input	**Over Current** for USB 2.0 ports

Group	Pins	Signal Name	Host Direction	Description
FBUS	2	FBUS_[0:1]RTS#	Output	**Ready To Send** output for Field Bus interfaces line drivers. Shifted when used.
	2	FBUS_[0:1]Tx(p)	Output	**Transmit or Differential Upper Line** for Field Bus interfaces. Shifted when used.
	2	FBUS_[0:1]Rx(n)	Input	**Receive or Differential Lower Line** for Field Bus interfaces. Shifted when used.
Stack Control	1	Type_DETECT#	Input	**Stack Type Detect** signal.100K pull-up to +3.3V_SB on HOST.
ATX Power Supply	1	PSON#	Output	**Power Supply On** brings the ATX power supply out of sleep mode. Open Drain on Host module.
	1	PWRGOOD	Input	**Power Good** from the power supply indicates that power is good. Open Drain on Power Source module.
	2	+5V_SB	Power	**Standby Power** for advanced power saving modes. Always on
	2	+5V	Power	**+5V** central power planes. Provided by Power Supply.
	2	+3.3V	Power	**+3.3V** power. Provided by Power Supply.
	1	+12V	Power	**+12V** central power plane. Provided by Power Supply.
	36	GND	Power	**GND** pins.
	1	GND (DIR)	Power	**GND** pin. Dedicated GND pin to implement compatibility with PCI/104-Express standard.
	1	RTC_Battery	Power	**Battery power** for stack modules, +3.3V
	[0:3] indicates link 0, 1, 2, or 3			
	[0:1] indicates link 0 or 1			
	# indicates “low level” active signals			

If Host module doesn’t implement some interfaces, corresponding pins should be left unconnected.

If Peripheral modules don’t use some interfaces, corresponding lines should pass through the stack connectors. It means that each unused pin on bottom connector should be connected to corresponding pin on top connector. Lines not having point-to-point nature like LPC, SMB, SPI (except SPI_SS[0:2]#), Type_DETECT#, DIR, STK[0:2] should be passed through by peripheral module no matter if they were used by this module or not.

STK0,1,2 must be pulled-up to +3.3V_SB or pulled-down to GND according to section B.3 PCIe/104.

Type_DETECT# must be pulled-up to +3.3V_SB on HOST.

+3.3V_SB should be obtained from +5V_SB Standby Power.

3. EXPANSION CONNECTOR B (PCI-104)

To support PCI/104-Express module with PCI bus there can be placed PCI-104 connector on the StackPC module. Information about PCI-104 connector can be found in PCI/104-Express specification.

StackPC modules with PCI-104 bus support called StackPC-PCI.

4. EXPANSION CONNECTOR B1 (FPE)

Expansion Connector B1 is the optional Fat Pipe Expansion connector targeting applications where high speed I/O or multimedia features are needed.

4.1. Functions

One 1x16 PCI Express interface which can be configured as 2x8 PCI Express, or 2x4 PCI Express
Display Port
Configurable Section
Power: +12V

4.2. Pin Assignment

Table 4-1 shows pin assignments for Connector B1 (FPE).

Table 4-1: Connector B1 (FPE) Pin assignments

Top View Signal Assignment of Connector B1 (FPE) (Profile 0)											
		ROWS									
		10	9	8	7	6	5	4	3	2	1
COLUMNS (EDGE OF THE BOARD)	1	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	AUX_CH+	HOT_PLUG
	2	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	AUX_CH-	GND
	3	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	DP_PWR	ML_L(1)p
	4	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	ML_L(3)p	ML_L(1)n
	5	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	ML_L(3)n	GND
	6	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	GND	ML_L(0)p
	7	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	Configurable	ML_L(2)p	ML_L(0)n
	8	Configurable	Configurable	Configurable	GND	Configurable	GND	Configurable	GND	ML_L(2)n	GND
	9	Reserved	Reserved	GND	PEx16_0T(6)p	GND	PEx16_0T(4)p	GND	PEx16_0T(2)p	GND	PEx16_0T(0)p
	10	Reserved	Reserved	PEx16_0T(7)p	PEx16_0T(6)n	PEx16_0T(5)p	PEx16_0T(4)n	PEx16_0T(3)p	PEx16_0T(2)n	PEx16_0T(1)p	PEx16_0T(0)n
	11	PE_RST#	GND	PEx16_0T(7)n	GND	PEx16_0T(5)n	GND	PEx16_0T(3)n	GND	PEx16_0T(1)n	GND
	12	GND	PEx16_x8_x4_0Clkp	GND	PEx16_0R(6)p	GND	PEx16_0R(4)p	GND	PEx16_0R(2)p	GND	PEx16_0R(0)p
	13	FPE_Bus_Err#	PEx16_x8_x4_0Clkn	PEx16_0R(7)p	PEx16_0R(6)n	PEx16_0R(5)p	PEx16_0R(4)n	PEx16_0R(3)p	PEx16_0R(2)n	PEx16_0R(1)p	PEx16_0R(0)n
	14	Config_Type0	GND	PEx16_0R(7)n	GND	PEx16_0R(5)n	GND	PEx16_0R(3)n	GND	PEx16_0R(1)n	GND
	15	Config_Type1	PEx16_x8_x4_1Clkp	GND	PEx16_0T(14)p	GND	PEx16_0T(12)p	GND	PEx16_0T(10)p	GND	PEx16_0T(8)p
	16	Config_Type2	PEx16_x8_x4_1Clkn	PEx16_0T(15)p	PEx16_0T(14)n	PEx16_0T(13)p	PEx16_0T(12)n	PEx16_0T(11)p	PEx16_0T(10)n	PEx16_0T(9)p	PEx16_0T(8)n
	17	Reserved	GND	PEx16_0T(15)n	GND	PEx16_0T(13)n	GND	PEx16_0T(11)n	GND	PEx16_0T(9)n	GND
	18	+12V	Reserved	GND	PEx16_0R(14)p	GND	PEx16_0R(12)p	GND	PEx16_0R(10)p	GND	PEx16_0R(8)p
	19	+12V	Reserved	PEx16_0R(15)p	PEx16_0R(14)n	PEx16_0R(13)p	PEx16_0R(12)n	PEx16_0R(11)p	PEx16_0R(10)n	PEx16_0R(9)p	PEx16_0R(8)n
	20	+12V	Reserved	PEx16_0R(15)n	GND	PEx16_0R(13)n	GND	PEx16_0R(11)n	GND	PEx16_0R(9)n	GND

4.3. Signal Descriptions

Table 4-2: Connector B1 (FPE) Signals

Group	Pins	Signal Name	Host Direction	Description
1x16, 2x8, or 2x4 PCIe Links	16 16 8	PEx16_0T(0:15)p PEx8_[0:1]T(0:7)p PEx4_[0:1]T(0:3)p	Output	**Transmit Differential Upper Lines** for the x16, x8 or the x4 Links. The x4 and x8 Links should be shifted when used.
	16 16 8	PEx16_0T(0:15)n PEx8_[0:1]T(0:7)n PEx4_[0:1]T(0:3)n	Output	**Transmit Differential Lower Lines** for x16, x8 or the x4 Links. The x4 and x8 Links should be shifted when used.
	16 16 8	PEx16_0R(0:15)p PEx8_[0:1]R(0:7)p PEx4_[0:1]R(0:3)p	Input	**Receive Differential Upper Lines** for the x16, x8, or the x4 Links. The x4 and x 8 Links should be shifted when used.
	16 16 8	PEx16_0R(0:15)n PEx8_[0:1]R(0:7)n PEx4_[0:1]R(0:3)n	Input	**Receive Differential Lower Lines** for the x16, x8, or the x4 Links. The x4 and x8 Links should be shifted when used.
	2	PEx16_x8_x4_[0:1]CLKp	Output	**Clock Differential Upper Line** for x16 or x8 or x4 Link.
	2	PEx16_x8_x4_[0:1]CLKn	Output	**Clock Differential Lower Line** for x16 or x8 or x4 Link.
PCIe	1	PE_RST#	Output	**Reset** for PCI Express Bus
DisplayPort	4	ML_L[0:3]p	Bidirectional	**Differential Upperr Line for Main Link Line** for Display Port.
	4	ML_L[0:3]n	Bidirectional	**Differential Lower Line for Main Link Line** for Display Port.
	1	AUX_CHp	Bidirectional	**Half-duplex AUX channel Positive Link** for Display Port.
	1	AUX_CHn	Bidirectional	**Half-duplex AUX channel Negative Link** for Display Port.
	1	DP_PWR	Power	**+3.3V Power** for Display Port
	1	HOT_PLUG	Input	**Hot Plug Detect** for Display Port
Configurable Section	61	Configurable	Configurable	**Configurable Section**. Pin out is Profile dependent.
	3	Config_Type[0:2]	Input	**Configuration Type.** Defines one of 8 possible pin outs for Configurable Section.
	1	FPE_Bus_Err#	Input	**FPE Bus Stacking Error.** Pull-up on Host.
Power Supply	3	+12V	Power	**+12V** power. Provided by Power Supply. The same as for StackPC connector
	43	GND	Power	**GND** pins. Additional GND pins may be defined in Configurable Section.
Reserved	8	Reserved		**Reserved** for future use
	# indicates the lane within a link			
	[0:3] indicates link 0, 1, 2, or 3			
	[0:1] indicates link 0 or 1			

Config_Type[0:2] lines must be pulled-up with 10K to +3.3V_SB or pulled-down to GND according to section APPENDIX C: Expansion Connector B1 (FPE) Configurable Section Profiles.

FPE_Bus_Err# must be pulled-up with 10K to +3.3V_SB on HOST.

+3.3V_SB should be obtained from +5V_SB Standby Power (Expansion Connector A).

4.3.1 PCI Express Links

4.3.1.1 x16 Link Alternate Uses

The x16 Link that available on FPE (Connector B1) is also able to be configured for alternate uses. These uses include two x8 Links, or two x4 Links. Support for these alternate modes is Host and Device dependent. A Host that supports an x16 Link is not required to support two x8, or two x4 Links. Also, a Device that supports operation at x16 is not required to support operation at x8 or x4.

4.3.1.2 x8 and x4 Links

Two x8 Links can be provided on the x16 Link. Each x8 Link may also be used as an x4 Link.

The pin assignments for the x8 and x4 Links are shown in Table 4-3 below.

Table 4-3: x16 Link as Two x8 or Two x4 Links

Host Transmit Signals			Host Receive Signals		
x16 Signal	x8 Signal	x4 Signal	x16 Signal	x8 Signal	x4 Signal
PEx16_0T(0)	PEx8_0T(0)	PEx4_0T(0)	PEx16_0R(0)	PEx8_0R(0)	PEx4_0R(0)
PEx16_0T(1)	PEx8_0T(1)	PEx4_0T(1)	PEx16_0R(1)	PEx8_0R(1)	PEx4_0R(1)
PEx16_0T(2)	PEx8_0T(2)	PEx4_0T(2)	PEx16_0R(2)	PEx8_0R(2)	PEx4_0R(2)
PEx16_0T(3)	PEx8_0T(3)	PEx4_0T(3)	PEx16_0R(3)	PEx8_0R(3)	PEx4_0R(3)
PEx16_0T(4)	PEx8_0T(4)		PEx16_0R(4)	PEx8_0R(4)	
PEx16_0T(5)	PEx8_0T(5)		PEx16_0R(5)	PEx8_0R(5)	
PEx16_0T(6)	PEx8_0T(6)		PEx16_0R(6)	PEx8_0R(6)	
PEx16_0T(7)	PEx8_0T(7)		PEx16_0R(7)	PEx8_0R(7)	
PEx16_0T(8)	PEx8_1T(0)	PEx4_1T(0)	PEx16_0R(8)	PEx8_1R(0)	PEx4_1R(0)
PEx16_0T(9)	PEx8_1T(1)	PEx4_1T(1)	PEx16_0R(9)	PEx8_1R(1)	PEx4_1R(1)
PEx16_0T(10)	PEx8_1T(2)	PEx4_1T(2)	PEx16_0R(10)	PEx8_1R(2)	PEx4_1R(2)
PEx16_0T(11)	PEx8_1T(3)	PEx4_1T(3)	PEx16_0R(11)	PEx8_1R(3)	PEx4_1R(3)
PEx16_0T(12)	PEx8_1T(4)		PEx16_0R(12)	PEx8_1R(4)	
PEx16_0T(13)	PEx8_1T(5)		PEx16_0R(13)	PEx8_1R(5)	
PEx16_0T(14)	PEx8_1T(6)		PEx16_0R(14)	PEx8_1R(6)	
PEx16_0T(15)	PEx8_1T(7)		PEx16_0R(15)	PEx8_1R(7)	

4.3.1 FPE Bus Stacking Error (FPE_Bus_Err#) Signal

This signal is pulled Low by StackPC-FPE peripheral module in case it detects Configurable Sections conflict (Configurable Sections with different Profile Numbers are connected). It is Pulled-up to +5V_SB on CPU module. If signal is not used by peripheral module it should be “pass through”.

5. OPTIONAL StackPC POWER CONNECTORS (StackPWR)

Optional StackPWR connectors provide power and power control signals to the Host board directly without using main data connectors. It simplifies designing power supply modules and reduces its cost. Defining standard locations and types of power connectors allows better compatibility of products from different vendors.

5.1. Functions

- +5V_SB, PSON#, POWERGOOD for ATX power management
- Power: +3.3V, +5V, +12V, -12V

5.2. Pin Assignment

Table 5-1: StackPWR connectors pinout

Group	Pins	Signal Name	Host Direction	Description
StackPWR-1	1	GND	Power	**GND** pin.
	2	GND	Power	**GND** pin.
	3	+5V	Power	**+5V** Power Supply rail.
	4	+5V	Power	**+5V** Power Supply rail.
StackPWR-2	1	GND	Power	**GND** pin.
	2	GND	Power	**GND** pin.
	3	GND	Power	**GND** pin.
	4	+3.3V	Power	**+3.3V** Power Supply rail.
	5	+12V	Power	**+12V** Power Supply rail.
	6	+12V	Power	**+12V** Power Supply rail.
StackPWR-3	1	+5V_SB	Power	**Standby Power** for advanced power saving modes. Always on.
	2	POWERGOOD	Input	**Power Good** from the power supply indicates that power is good.
	3	PSON#	Output	**Power Supply On** brings the ATX power supply out of sleep mode.
	4	GND	Power	**GND** pin.

5.3. Mounting Options

There are 2 main options for using Power connectors:

1) Placing vertical power connectors on Bottom side of Host module. It allows connecting power supply module (with matching power connectors on its Top) from Bottom side of Host module in the same stackable board-to-board style as for regular data connectors (see Figure 6-6 and section 8.6.APPENDIX D:). Cable connection also can be used. It's recommended to use connectors described in section 8.4.

2) Placing vertical or angled connectors on Top side of Host module for connecting external power supply via cables. In this case any type of power connectors can be used that matches board height requirements.

It is not necessary to reroute Host module to use different options since all of them use the same Host board layout.

StrackPWR-1 power connector is used for providing +5V to the system.

StackPWR-2 power connector is used for providing +3.3V and +12V to the system.

StackPWR connectors can deliver enough power even for high performance CPU and Peripheral modules. Host board may be designed to use one of power connectors or both of them depending from requirements.

StackPWR-3 connector is used for ATX power control signals and for +5V_SB Power.

6. STACKING

6.1. Host and Peripheral Modules relative position in the Stack

StackPC specification defines only Stack-Up configuration for StackPC and FPE connectors. It means that Host board should be always the “first” in StackPC basic connector stack. It does not affect system level flexibility because in particular application CPU module can be out most left, right, top or bottom module in stack depending from the whole stack orientation, while microprocessor can be located on top or bottom side of CPU module depending from system cooling approach.

“Stack-Up only” configuration simplifies peripheral modules design since bus signal switches needed in case of bi-directional stack concept are not required. As a result peripheral boards can get advantages in available PCB real-estate, cost, power consumption, and signals integrity. It also allows avoiding StackPC and FPE connectors on bottom side of CPU modules giving more PCB real estate for implementing extra functionality and allowing more standardized and cost effective heat sink solutions.

At the same time, PCI/104 legacy modules can be used with StackPC-PCI CPU modules in Stack-Down fashion. StackPC specification also doesn’t limit using PCIe/104 Type 1 or Type 2 connectors on bottom side of CPU module thus allowing mixed Stack-Up/Stack-Down configuration with CPU module being in the middle of the stack.

6.2. StackPC Stack-Up Link Shifting

StackPC uses the same Link Shifting concept as defined in PCIe/104 specification. Host should connect DIR signal (Pin 45 of Connector A) to GND plane that according to PCIe/104 specification means “Stack-Up”. StackPC peripheral modules pass through DIR signal and may use it to detect wrong Stack-Down stacking. PCIe/104 peripheral modules pass through DIR signal and use it to detect stack direction. Thus StackPC provides compatible with PCIe/104 implementation of “Stack-Up only” concept. Link shifting is utilized so that peripheral modules can be built uniformly and consistently while using dedicated point-to-point connections.

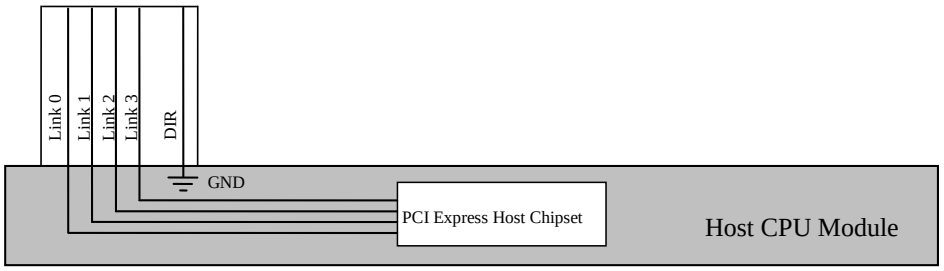


Figure 6-1: StackPC Host Module always configured as a “bottom” module in stack.

Since StackPC peripheral modules are always above the Host CPU Module, peripheral modules should always use lowest number Link first.

Figure 6-2 shows example of peripheral module using one PCIe Link.

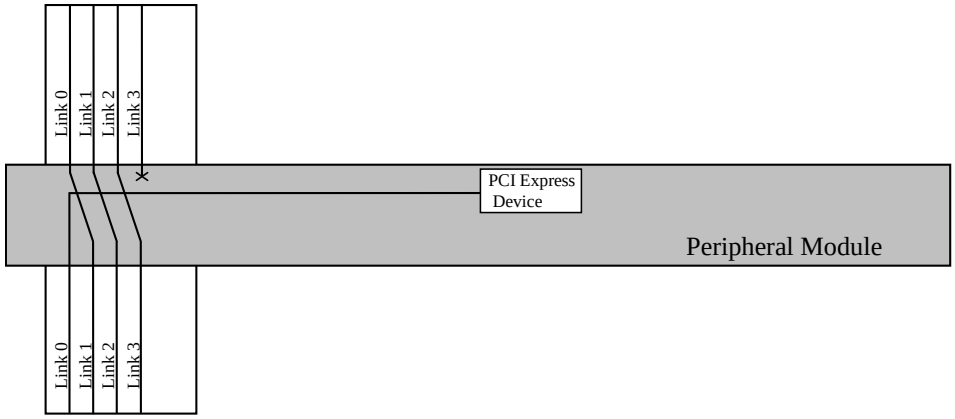


Figure 6-2: StackPC Peripheral Module Link Shifting

In this case Link 0 is connected to the PCIe device. Links 1, 2, and 3 are shifted and passed over so that Link 1 is in the Link 0 position, Link 2 is in the Link 1 position, and Link 3 is in the Link 2 position. A left-most Link is now available for the next peripheral module to be stacked above the first one.

The same principle is used for shifting other StackPC interfaces.

Connector A (StackPC) contains the following Shiftable Link Groups: 4x1 PCIe Link Group, USB Group (USB ports 0,1,2,3,4,5), SATA Group (ports 0,1), Ethernet Group (ports 0,1), SPI Group (SS# 0,1,2), FieldBus Group (FBUS ports 0,1).

There is only one Link for 1x4 PCIe, LPC and SMBus interfaces therefore Link Shifting is not applicable to them.

Connector B1 (FPE) supports two PCIe x8/x4 shiftable links. If PCIe x16 configuration is used then PCIe Link shifting on FPE connector is not applicable.

When a module uses one of the x8/x4 Links, the other Link is shifted according to the same rule as for x1 Links on Connector A (StackPC).

Configurable section of FPE connector may have shiftable and/or not shiftable links depending on particular configuration.

6.2.1 PCB Link Shifting

As a demonstration of link shifting in the presence of multiple link groups, the x1 PCIe, USB, SATA and FBUS groups are used in Figure 6-3: Link Shifting Examples for Host and Various Peripheral Modules. Any peripheral module may use one or more Links. If multiple Links are used then a necessary link shifting must be implemented on the module PCB for each Link and Link Group. For example, in the case where two x1 PCIe Link devices are resident on the module, it is required that the remaining two unused Links should be shifted two locations in order to make other modules able to use the remaining Links. It is not enough to shift only one link space as in the case of module having only one x1 PCIe Link Device.

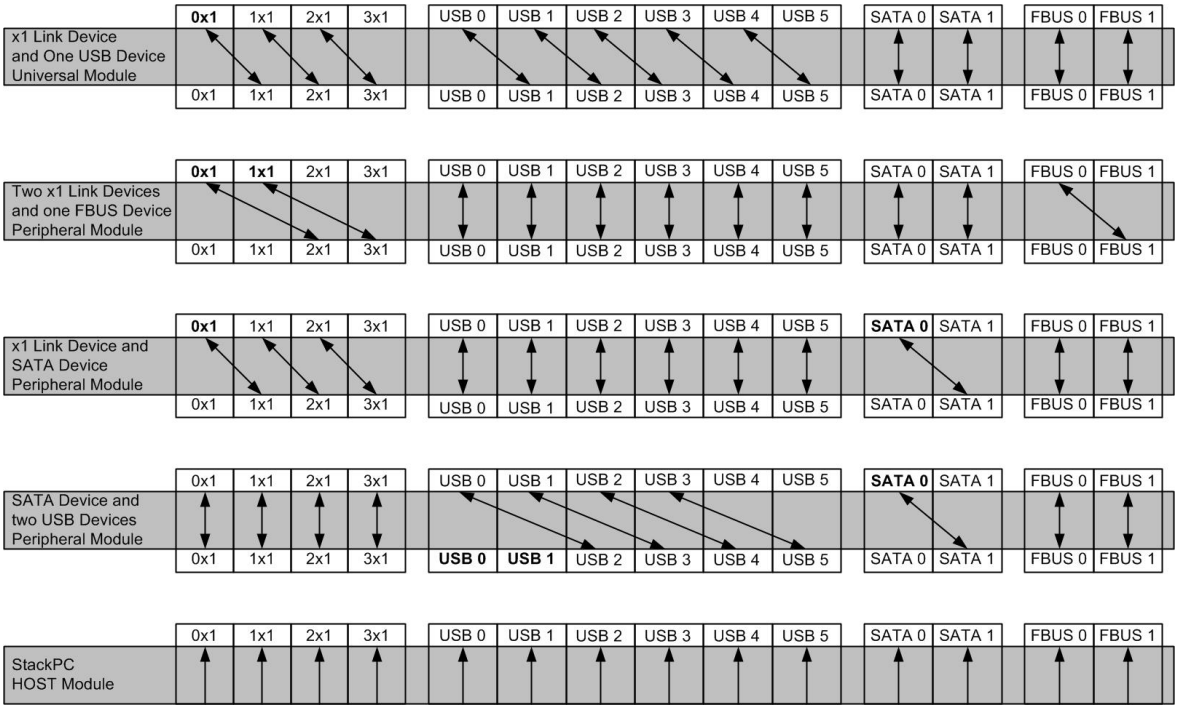


Figure 6-3: Link Shifting Examples for Host and Various Peripheral Modules

6.2.2 Link Shifting Stack Examples

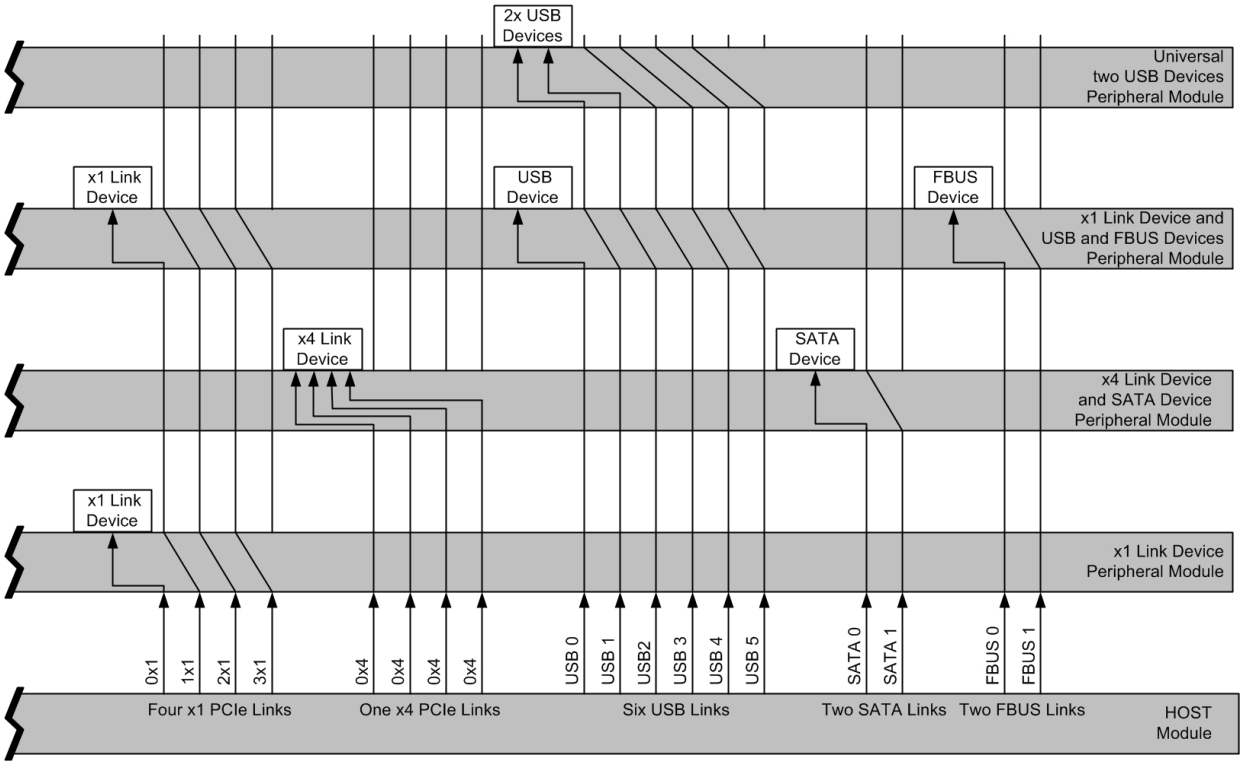


Figure 6-4: Automatic Link Shifting Stack-Up Example with PCIe, USB, SATA and FBUS interfaces.

6.3. System Stacking Rules

A PCI Express Link may only traverse up to six stacked connectors height (StackPC or FPE).

A PCI bus may only traverse up to four stacked PCI connectors, and they must all be on the same side of the Host. Because of the requirements of trace length matching, all PCI Devices must be stacked together and must be next to the Host.

6.4. Stack Configuration Examples

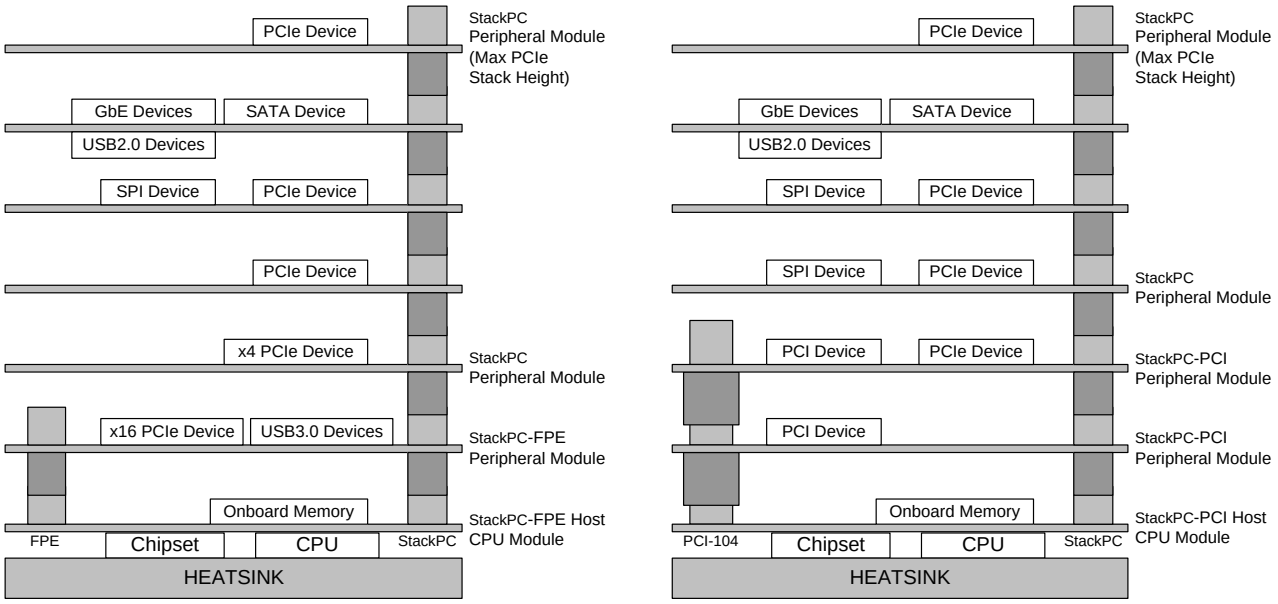


Figure 6-5: Stack-Up Configuration Examples for StackPC-FPE and StackPC-PCI.

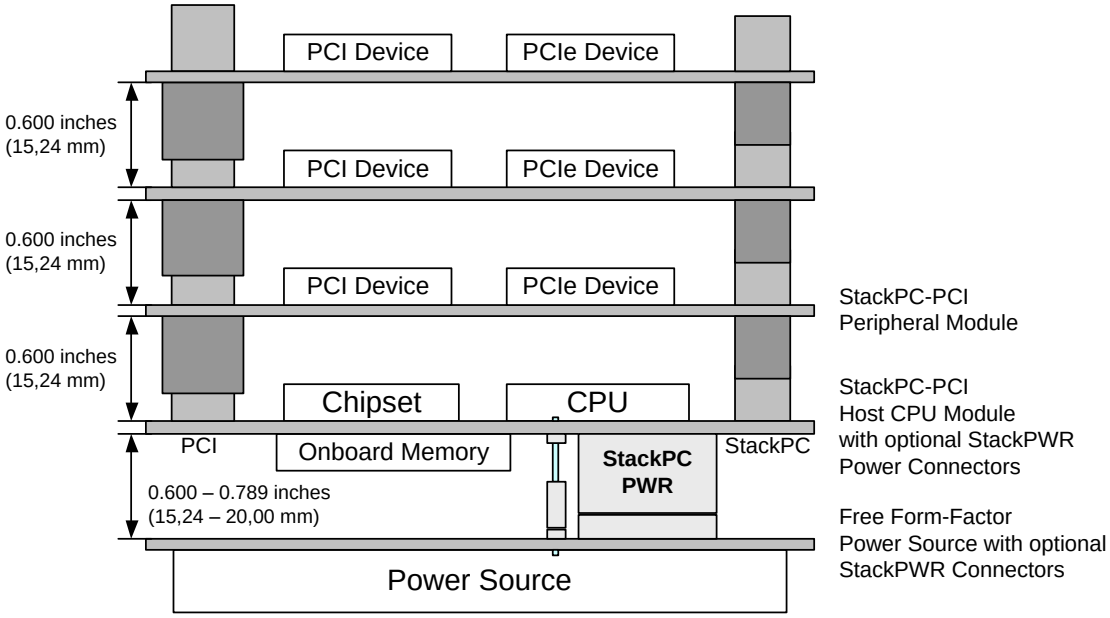


Figure 6-6: Stack-Up Configuration Example Using Power Module with StackPWR Connectors

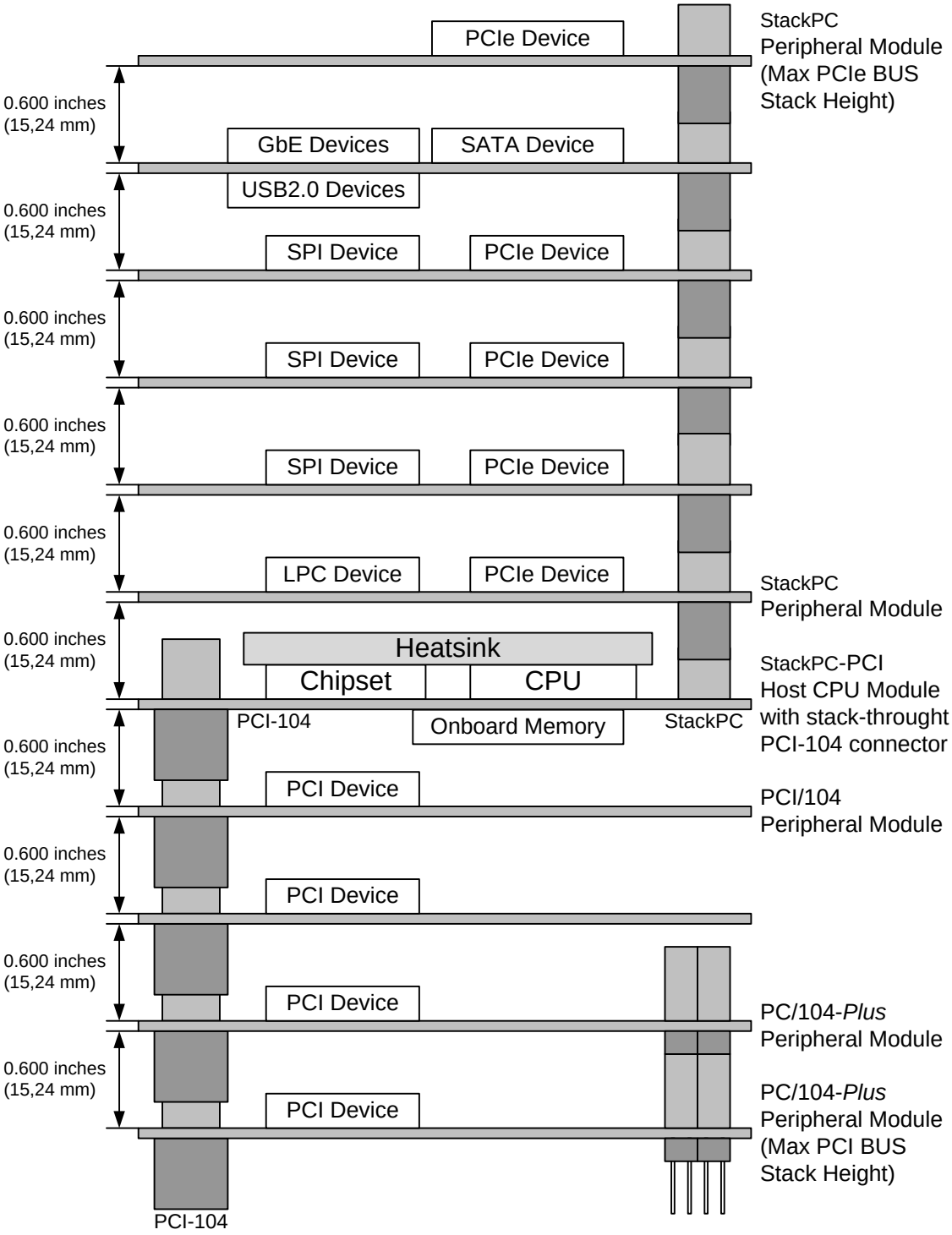


Figure 6-7: Combined Stack-Up and Stack-Down Configuration Example

7. ELECTRICAL SPECIFICATION

7.1. Power and Ground

7.1.1 Connector A (StackPC) Power Capabilities

Power on Connector A comes from +5V_SB, +3.3V, +5V, and +12V. The +5V and +12V are carried on central conductor planes which are dispersed among the three banks of Connector A. The +5V_SB and +3.3V are carried on individual pins. The current carrying capacities of the central panes and pins are shown in Table 7-1 below. Current values include a 20% industry standard de-rating factor at 85 · C. Note that at lower temperatures the current carrying capacities increase.

Table 7-1: Connector A (StackPC) Power Delivery

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Number of Pins	Current per Pin (A)	Total Current (A)	Total Power (W)
+3.3V	3.0	3.6	2	1.8	3.6	11.9
+5V	4.75	5.25	2 planes	8.4	16.8	84.0
+5V_SB	4.75	5.25	2	1.8	3.6	18.0
+12V	11.40	12.60	1 plane	8.4	8.4	100.8
GND	n/a	n/a	37	1.8	66.6	n/a

Current values are shown for +85ºC ambient temperature.

Standby power (+5V_SB) is supplied for “wake up” capabilities. Because of the limited amount of power available during standby, it is important for StackPC modules to be designed to minimize power consumption from the standby rail. Note that during full power operation, the voltage on the Standby rail may exceed the voltage on the +5V rail. Therefore, if devices are powered from both the standby and the +5V rail, care must be taken not to exceed the current limits of the Standby rail during normal operation.

7.1.2 Connector B1 (FPE) Power Capabilities

Table 7-2: Connector B1 (FPE) Power Delivery

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Number of Pins	Current per Pin (A)	Total Current (A)	Total Power (W)
+12V	11.40	12.60	3	1.75	5.25	63
GND	n/a	n/a	>=43	1.75	>=75.25	n/a

Current values are shown for +60ºC ambient temperature.

7.1.3 StackPWR Connectors Power Capabilities

Table 7-3: StackPWR Connectors Power Delivery.

Voltage	Minimum Voltage (V)	Maximum Voltage (V)	Number of Pins	Current per Pin (A)	Total Current (A)	Total Power (W)
+3.3V	3.00	3.60	1	5.5	5.5	18.15
+5V	4.75	5.25	2	5.5	11	55.0
+5V_SB	4.75	5.25	1	2.5	2.5	12.5
+12V	11.4	12.6	1	5.5	5.5	66.0
GND	n/a	n/a	5	5.5	27.5	n/a
GND	n/a	n/a	1	2.5	2.5	n/a

Current values are shown for +85ºC ambient temperature.

Power and ground planes are shared among all of the Expansion Connectors and StackPWR connectors. In case if power source is connected to the stack via one of available connectors then total power available for each power rail is limited by that connector. To provide more power to the system power supply can use more than one connector for delivering power.

7.2. AC/DC Signal Specifications

7.2.1 Stackable PCI Express Expansion Bus

For full details on the electrical requirements for the PCIe bus, please, refer to the *PCI Express Base Specification,* referenced in Section 1.7.

7.2.2 Stackable PCI Expansion Bus

For full details on the electrical requirements for the stackable PCI bus, please, refer to the *PC/104-Plus* or *PCI-104 Specifications,* referenced in Section 1.7

7.2.3 Gigabit Ethernet

For full details on electrical requirements for Gigabit Ethernet, please, refer to *IEEE 802.3 Ethernet Standard*, referenced in Section 1.7. In case if used Ethernet controller brings specific requirements it should be described in User Manual.

7.2.4 USB, SATA, LPC, SPI, SMBus

For full details on the electrical requirements, please, refer to the appropriate standard or specification referenced in Section 1.7.

8. MECHANICAL SPECIFICATIONS

8.1. Connector A (StackPC)

Samtec's QMS/QFS High Speed Interface series connectors were optimized for 0.600 inch (15.24mm) stacking height and standoff tolerances. An equivalent connectors can be used.

Host Modules use only Top Connectors for StackPC while Peripheral Modules use both Top and Bottom Connectors. If peripheral module is designed as a last (Top) module in the stack it can omit Top connector. Optional Top connector with 22mm height can be used instead of 15.24mm version if more space is required above the board.

8.1.1 Part Number

Top Connector (Standard):	ASP-129637-03 with 0.600 inch (15.24 mm) stack height
Top Connector (Optional):	ASP-142781-03 with 0.866 inch (22.00 mm) stack height
Bottom Connector (Standard):	ASP-129646-03 with 0.600 inch (15.24 mm) stack height

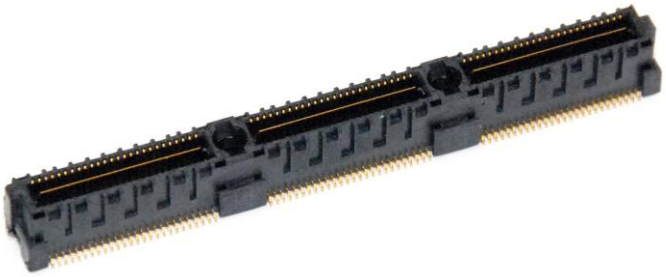


Figure 8-1: Top Connector ASP-129637-03 or equivalent

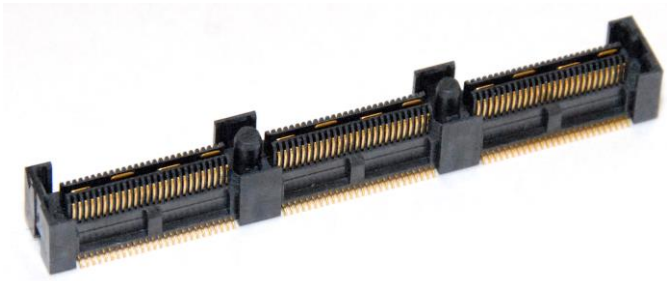
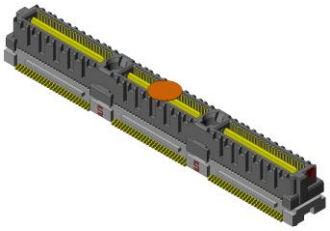
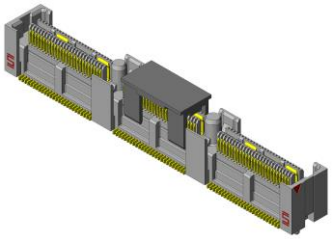


Figure 8-2: Bottom Connector ASP-129646-03 or equivalent





Top Connector **Bottom Connector**

Figure 8-3: Top Half and Bottom Half Connectors shown with Pick-and-Place Adapters

8.1.2 Connector A (StackPC) Specifications

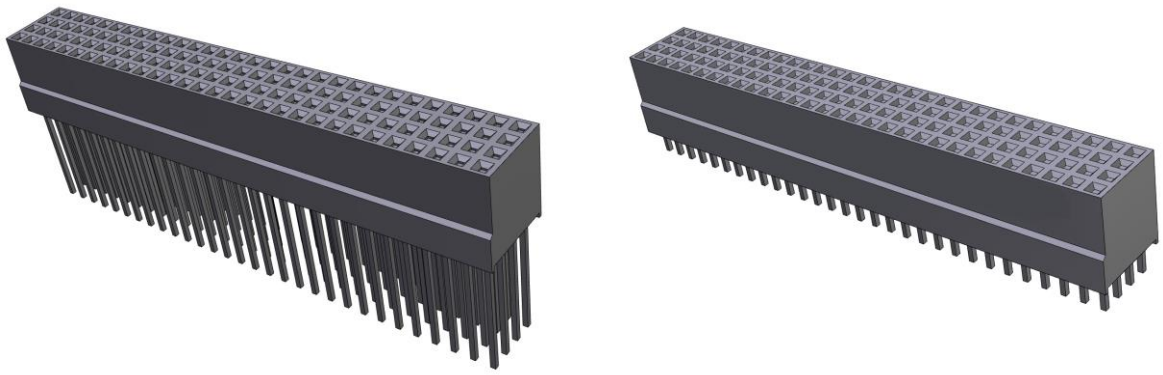
MATERIALS	
Housing:	Liquid Crystal Polymer
Terminal & Ground Plane Material:	Phosphor Bronze
Terminal Plating:	Au over 50· ” (1.27· m) Ni
Plane Plating:	Au over 50· ” (1.27· m) Ni
Terminal and Plane Tails:	Tin
CONTACT FINISH	
Socket Interface:	30· ” Au
Terminal Interface:	30· ” Au
Underplate:	50· ” Ni
MECHANICAL PERFORMANCE	
Insertion Force:	13.9 lbs initial & 16.8 lbs @ 100 cycles
Withdrawal Force:	9.8 lbs initial & 10.0 lbs @ 100 cycles
Normal Force @ nominal deflection:	69 grams
Minimum stacking size:	14.8mm
Nominal stacking size:	15.24mm
Maximum stacking size:	15.50mm
Contact wipe (at nom. Height):	.044” [1.22mm]
Ground Plane wipe (at nom. Height):	.059” [1.50mm]
Durability:	50 cycles
Operating Temp:	-55· C to 125· C
ELECTRICAL PERFORMANCE	
Positions	Three banks of 52 pins and 1 plane for 156 total pins and 3 planes
Contact Resistance (initial):	30 mOhms

Contact Resistance (@ 1,000 cycles):	50 mOhms
Contact Current Capacity:	1.8A at 85・C and with 20% Industry Standard Derating Factor
Ground Plane Resistance:	0.5 mOhms
Ground Plane Current Capacity:	8.4A at 85・C and with 20% Industry Standard Derating Factor
Dielectric Withstanding Voltage:	900 VAC
Working Voltage:	300 VAC
Insulation Resistance:	50,000 megaOhms
SOLDERABILITY	
Maximum Processing Temperature:	230・C for 60 seconds or 260・C for 20 seconds
HIGH FREQUENCY PERFORMANCE	
Differential Pair Impedance	100 Ohms nominal +/- 10%
Single-Ended Impedance	50 Ohms nominal +/- 10%
Differential Return Loss (SDD11):	-15dB @ 1.25 GHz; -8dB @ 5 GHz
Differential Insertion Loss (SDD21):	-1dB @ 1.25 GHz; -3dB @ 5 GHz
Differential Near End Crosstalk (SDD31):	-45dB @ 1.25 GHz; -35dB @ 5 GHz
Differential Far End Crosstalk (SDD41):	-45dB @ 1.25 GHz; -25 dB @ 5 GHz

8.2. Connector B (PCI-104)

Connector B is the standard PCI bus connector used on PC/104-Plus and PCI-104 modules. See the PC/104-Plus or PCI-104 Specification for mechanical specification of the connector.

Host Modules should use Non-Stackthrough PCI-104 connector and Peripheral Modules should use Stackthrough connector.



Stackthrough Non-Stackthrough

Figure 8-4: Stackthrough and Non-Stackthrough PCI-104 connectors

8.3. Connector B1 (FPE)

The SEAF/SEAM series connectors from Samtec's High Speed/High Density Open Pin Field connectors are used as Fat Pipe Expansion (FPE) connector for high bandwidth and multimedia interfaces.

Host Modules should use only Top Connectors while Peripheral Modules may use both Top and Bottom Connectors. If peripheral module is designed as a last (Top) module in the stack it can omit top connector.

8.3.1 Connector B1 (FPE) Part Number

Top Connector:	SEAF-20-06.0-L-10-2-A-K-TR with 0.600 inch (15.24 mm) stack height
Bottom Connector:	SEAM-20-09.0-L-10-2-A-K-TR with 0.600 inch (15.24 mm) stack height

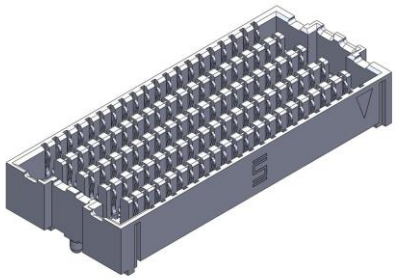


Figure 8-5: Top Connector SEAF-20-06.0-X-10-2-A

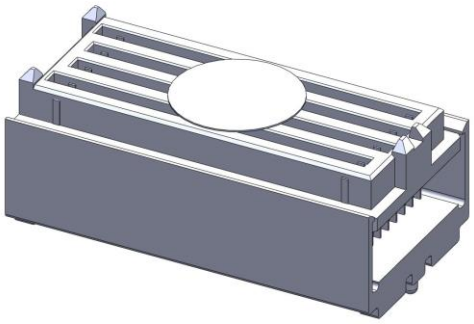


Figure 8-6: Bottom Connector SEAM-20-09.0-X-10-2-A

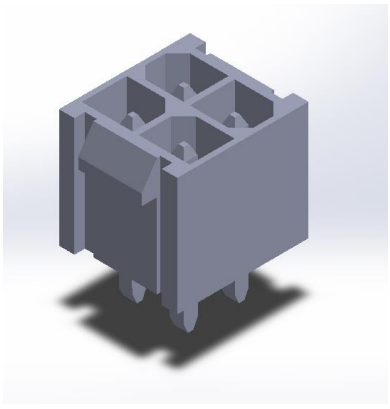
8.3.2 Connector B1 (FPE) Specifications

MATERIALS	
Housing:	Black Liquid Crystal Polymer
Contact:	Copper Alloy
Contact Plating:	Au over 50· ” (1.27· m) Ni
CONTACT FINISH	
Socket Interface:	10-30· ” Au
MECHANICAL PERFORMANCE	
Maximum Maiting Force:	36 lbs
Minimum Unmating Force:	16.1 lbs
Normal Force @ nominal deflection:	63 grams
Nominal stacking size:	15mm
Operating Temp:	-55· C to 125· C
ELECTRICAL PERFORMANCE	
Positions	10 rows of 20 pins per row for 200 total pins
Contact Resistance:	6.9 mOhms
Contact Current Capacity:	2.3A for a 20· C temp rise
Dielectric Withstanding Voltage:	900 VAC
Working Voltage:	240 VAC
Insulation Resistance:	>25,000 megaOhms

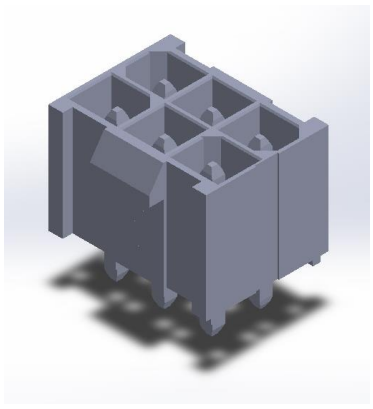
8.4. StackPC Power Connectors (StackPWR)

StackPC Power connectors are described in Section 5. Following part numbers of Samtec’s connectors are recommended for use as StackPC Power Connectors:

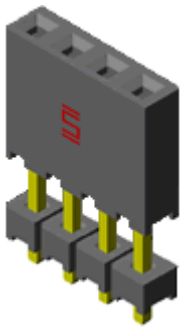
StackPWR-1 Host Bottom Connector:	IPBT-102-H1-X-D
StackPWR-2 Host Bottom Connector:	IPBT-103-H1-X-D
StackPWR-3 Host Bottom Connector :	ESQT-104-02-F-S-510
StackPWR-1 Power Module Top Connector:	IPBS-102-01-X-D
StackPWR-2 Power Module Top Connector:	IPBS-103-01-X-D
StackPWR-3 Power Module Top Connector :	TMM-104-03-L-S
Power Cable Housing for StackPWR-1 connector :	IPBD-02-D
Power Cable Housing for StackPWR-3 connector :	IPBD-03-D



StackPWR-1 (IPBT-102-H1-X-D)

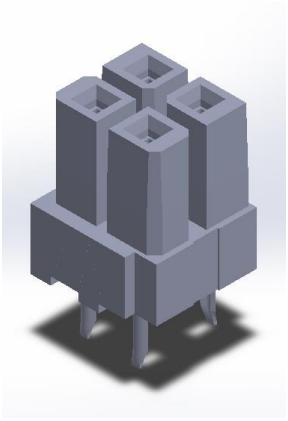


StackPWR-2 (IPBT-103-H1-X-D)

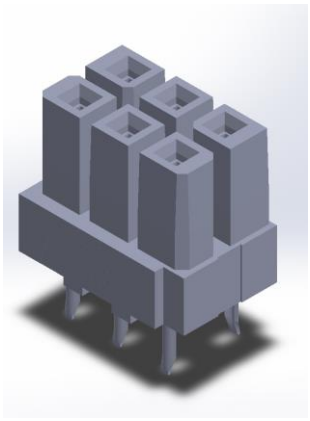


StackPWR-3 (ESQT-104-02-F-S-510)

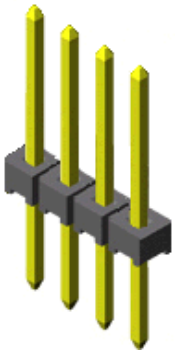
Figure 8-7: Host StackPWR Connectors



StackPWR-1 (IPBS-102-01-X-D)

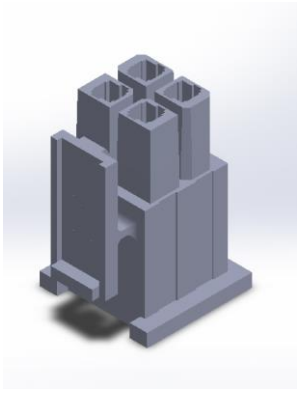


StackPWR-2 (IPBS-103-01-X-D)



StackPWR-3 (TMM-104-03-L-S)

Figure 8-8: Power Module StackPWR Connectors



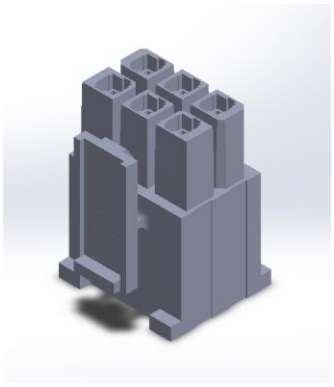


Figure 8-9: Power Source StackPWR-1 and StackPWR-2 Cable connectors

8.5. Standoffs

It's recommended to use standard 0.600 inches (15.24 mm) standoffs with outer diameter less than recommended standoff pad on the PCB 0.250 inches (6.35 mm).

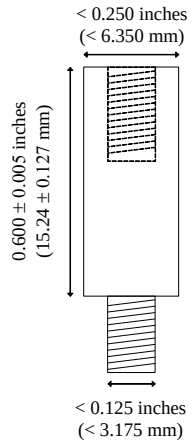


Figure 8-10: Standoff Mechanical Dimensions

8.6. StackPC Layout & Dimensions

This section describes layouts and dimensions for StackPC connectors. Current specification define only StackPC, FPE, StackPWR connectors relative position and doesn't define strict board dimensions. If adopting StackPC approach to other standards then board and mounting holes dimensions, component heights should be taken from appropriate specification.

Specification defines connectors layout and dimensions. These connectors layout can be easily adopted to most of popular form-factors like PCI/104-Express, EPIC, EBX, 3,5" and others.

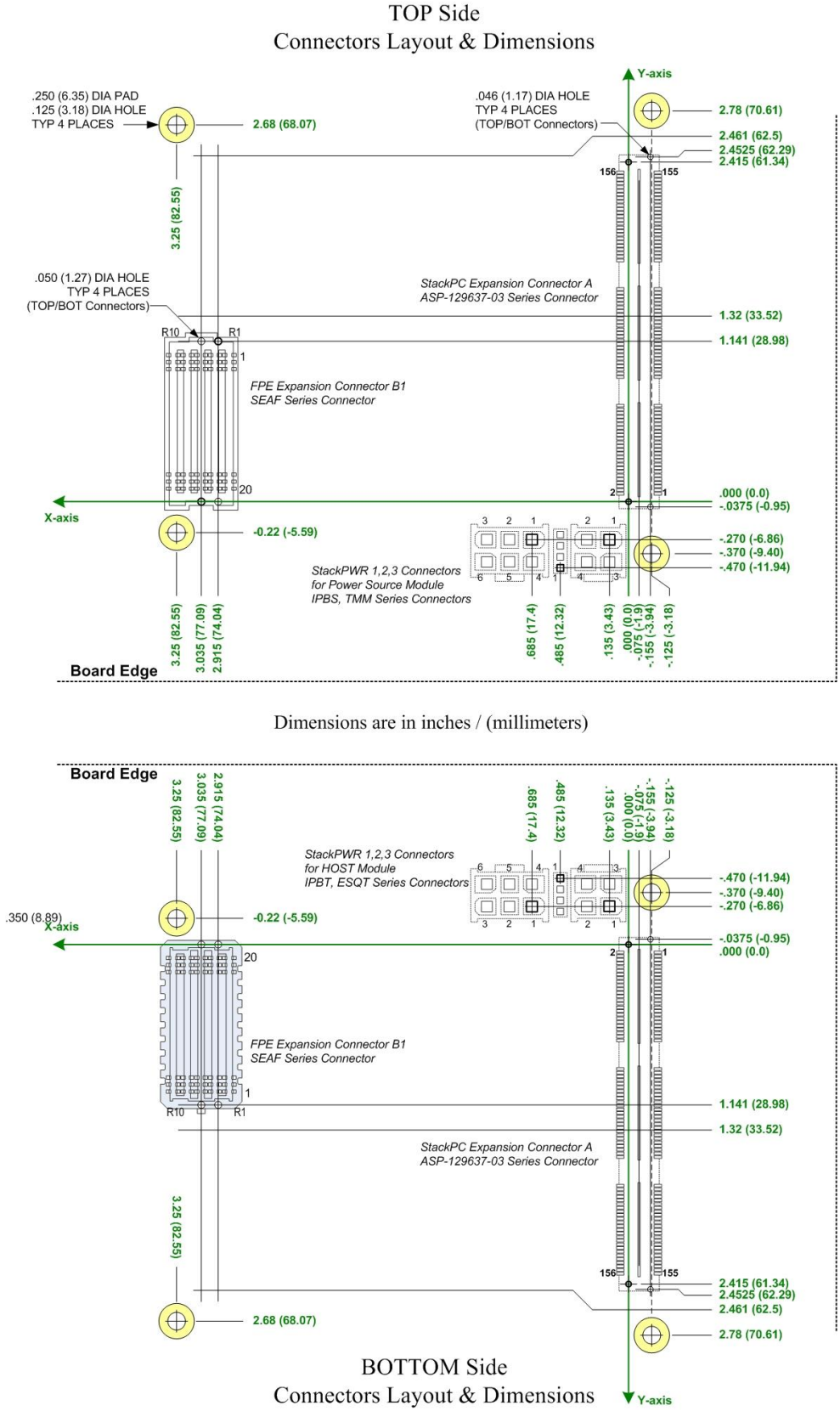


Figure 8-11: StackPC Layout & Dimensions

APPENDIX A: Layout and Routing Recommendations

Below are basic layout recommendations for PCI Express as a key high speed interface of StackPC specification. Additional requirements for PCI Express, USB, SATA, Gigabit Ethernet and other interfaces can be found in Layout Recommendations for particular Devices used on Host or Peripheral modules.

Due to PCI Express high data rate PCB layout becomes very critical. Therefore, the following recommendations should be followed to avoid signal integrity problems:

- Route all PCI Express signal lines (Transmit and Receive) as controlled impedance lines: 90 Ohm[1] for differential pairs and 55 Ohm for single ended traces.
- The clearance between a link and its neighbor must be at least 20 mils in the main routing region, 15 mils for stripline breakout, and 12 mils for microstrip breakout.
- Symmetrical routing must be used between the two signals of a differential pair.
- Signals in a differential pair must be matched to within 5 mils.
- AC coupling capacitors must be provided on the TX lines. Values should be between 75nF and 200nF. A surface mounted capacitor must be used.
- All PCI Express signals should be routed in an adjacent layer to a ground plane.
- Min 40-mil trace edge-to-major plane edge spacing
- No routing over plane splits. No routing over voids.
- Test Point and Probing (see Figure 8-12).
- No stubs except the short stub caused by the unused end of the Host connector. SI testing has shown this very short stub to be insignificant in a system with a Host and 6 add-in cards.
- Do not use 90 degree bends. Use 45 degree bends or curves.

[1] According to last recommendations of Intel Corp.

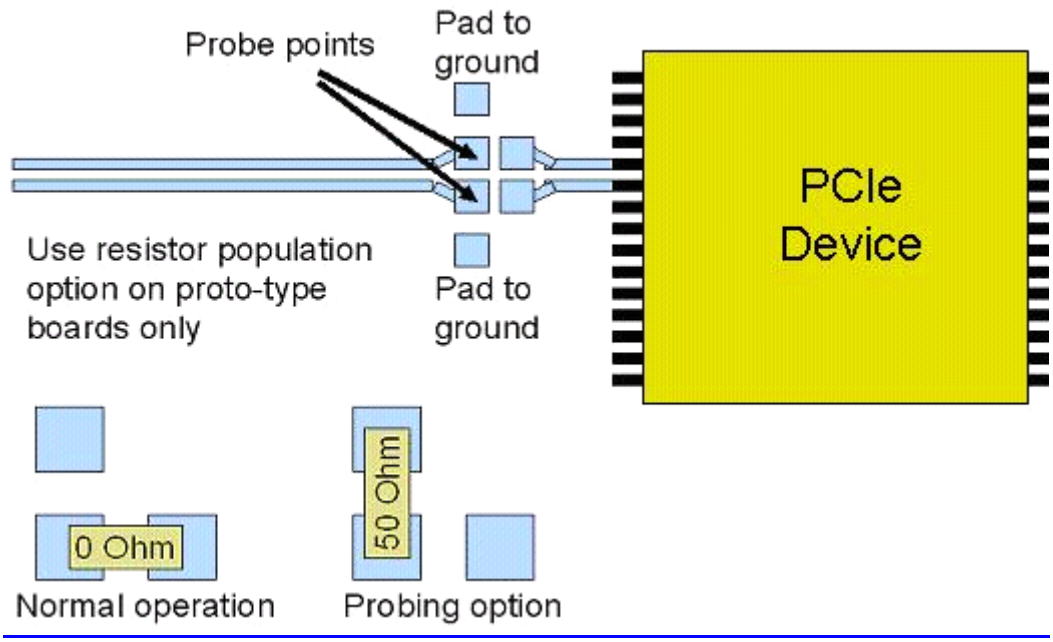


Figure 8-12: Test point and probing for PCIe link

Table 8-1: Via and Trace length budget

Location	Max. Vias	Max. Trace Length	Notes
Host TX lines	4	6000 mils	Both sides of AC cap.
Host RX lines	2	6000 mils	
Device TX Lines	4	4000 mils	Both sides of AC cap.
Device RX lines	4	4000 mils	
Pass-through (link shifting)	2	1000 mils	Includes stack height

A.1 Routing Topology

Figure 8-13: Capacitor placement below shows the positioning of the DC blocking capacitor and PCI Express connector in relation to the Host and Device. The DC blocking capacitor is placed on the transmit signals. This will be the signals the Host drives onto the Tx bus connector's pins and the signals the Device drives onto the Rx signals of the connector. The actual position is not critical; however the position must be closely matched between the signals of a differential pair.

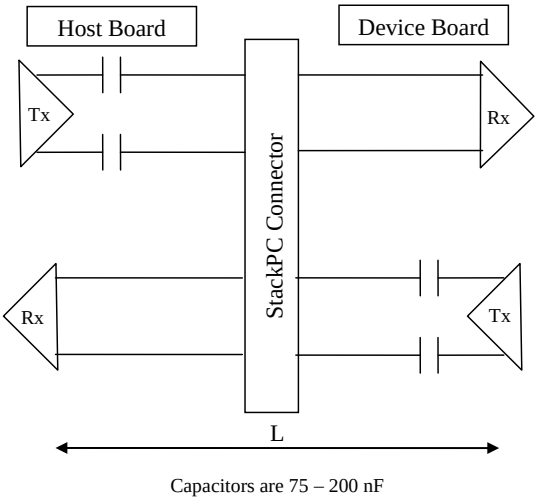


Figure 8-13: Capacitor placement

Table 8-2 below lists the general guide lines for PCI Express routing.

Table 8-2: PCI Express routing specification

Interface	Single Ended Impedance (Ohm)	Differential Impedance (Ohm)	Matching in a pair mil (mm)	Matching pair to pair mil (mm)
PCI Express	55 ±15%	90 ±20%	5 (0.127)	Not required

A.2 Microstrip Example

Typical trace dimensions for a microstrip over a ground layer are shown in Table 8-3 and Figure 8-14 below. The actual trace dimensions are dependent on layer stack-up. The dimensions should be chosen to result in a differential impedance of 90 Ω and a single ended impedance of 55 Ω. Microstrip technology is used on outer layers.

Table 8-3: Typical Trace dimensions for microstrip with FR4

Units	Nom. Trace Width	Nom. Trace Space	Pair to Pair Space	Insulator Thickness	Trace Thickness
	A	B	C	D1	T
mil	5	7	20	3.5 – 5.5	1.4 – 2.6

mm	0.127	0.178	0.508	0.089 – 0.140	0.036 – 0.066

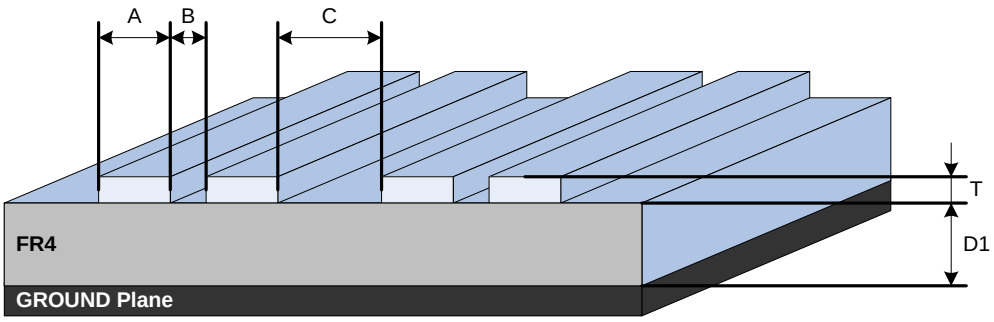


Figure 8-14: MicroStrip example

A.3 Stripline Example

Typical trace dimensions for a stripline are shown in Table 8-4 and Figure 8-15 below. The actual trace dimensions are dependent on layer stack-up. The dimensions should be chosen to result in a differential impedance of 90 Ω and a single ended impedance of 55 Ω. Stripline technology is used on inner layers.

Table 8-4: Typical Trace dimensions for stripline with FR4

Units	Nom. Trace Width	Nom. Trace Space	Pair to Pair Space	Insulator Thickness	Insulator Thickness	Trace Thickness
	A	B	C	D1	D2	T
mil	4	7	20	3.5 – 5.75	6 – 14	1.1 – 1.3
mm	0.102	0.178	0.508	0.089 – 0.146	0.152 – 0.356	0.028 – 0.033

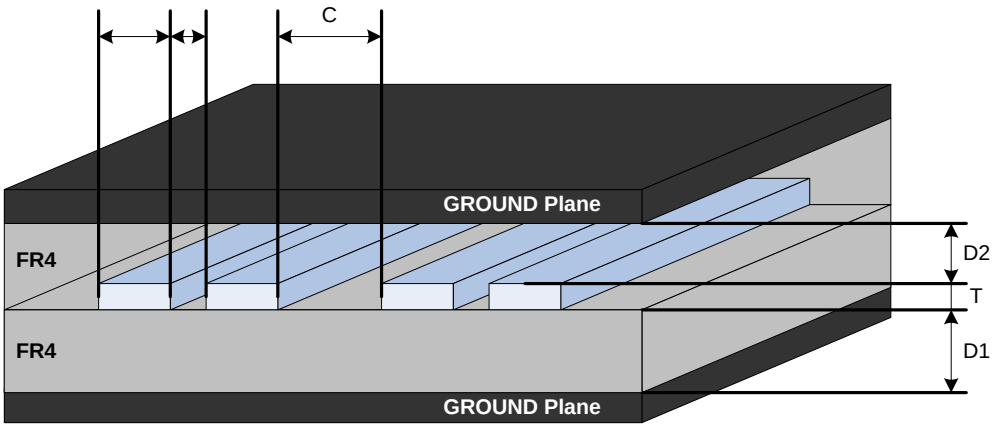


Figure 8-15: Stripline example

A.4 Device connector Break-Out Example

Figure 8-16 below shows an example of the routing from the Device connector to a x1 PCI Express Link Device. This drawing is not to scale and does not show controlled impedance lines. It is intended to show the general connections and link shifting on a device for a x1 PCI Express link that can be stacked above the Host module.

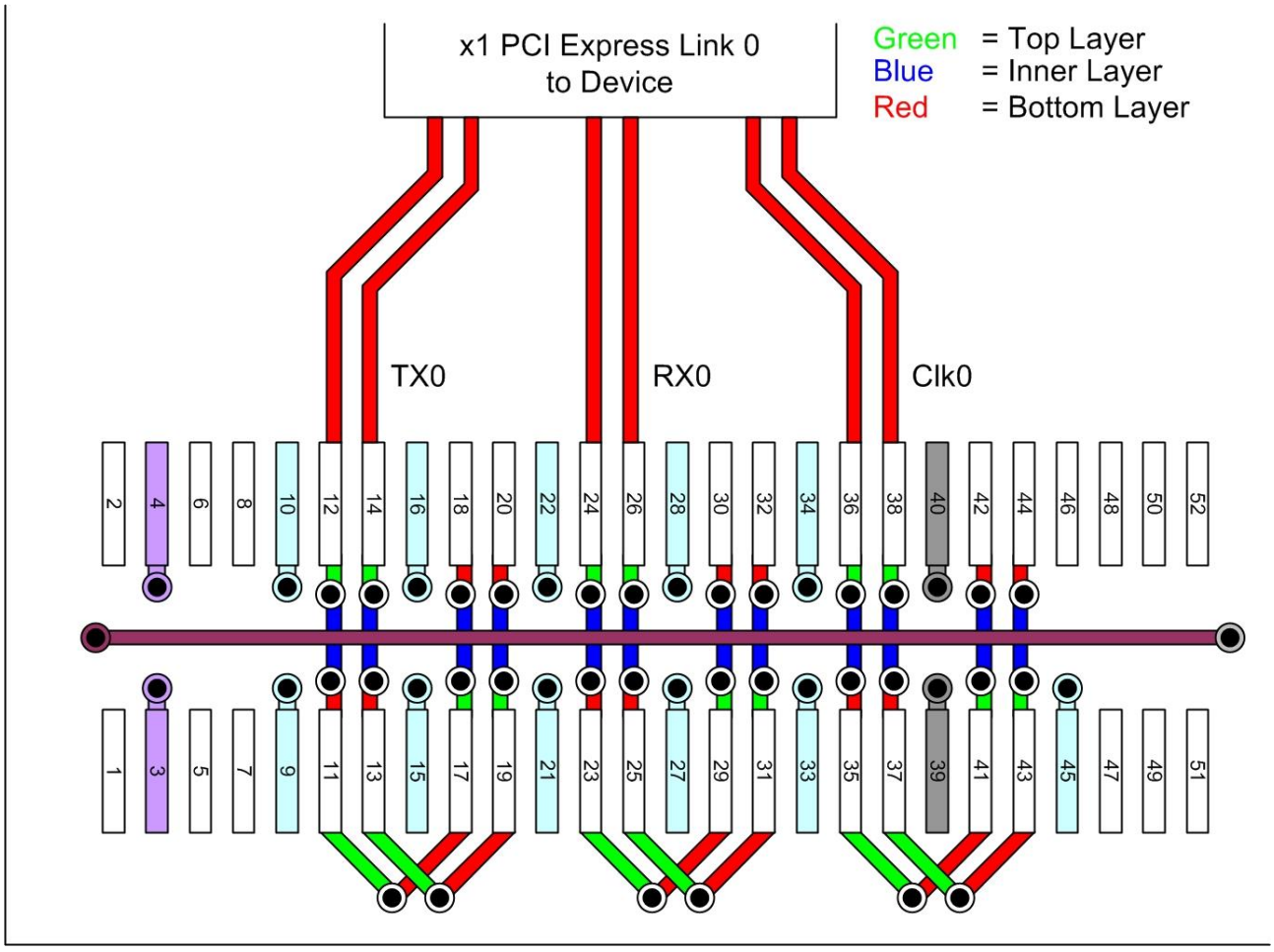


Figure 8-16: Example for break-out routing of connector Bank 1 from bottom to top with shifting.

APPENDIX B: Compatibility with PC/104 family of standards.

StackPC form factor is identical with PCIe/104 and PCI/104-Express in terms of mechanical dimensions, connector types, location of mounting holes and connectors. The difference is that StackPC specification does not define third “I/O Connectors overhang area” near Connector A.

Set of most important interfaces and its pin outs in most cases are also compatible. In the same time if StackPC and PC/104 modules are going to be mixed in one system there are some considerations which should be taken into account. Compatibility of StackPC with various PC/104 series standards is explained below.

B.1 PC/104 (ISA)

StackPC does not support directly ISA bus. Special adapter module with PCI-to-ISA bridge is required if PC/104 or PC/104-Plus modules should be used in StackPC system. For particular PC/104 module compatibility it is important to check whether adapter card brings any limitations on ISA bus functionality such as IRQ and DMA support.

The PCI-to-ISA Bridge module has three possible configurations: Basic, Stack-Up only, and Stack-Down only. If it is stacked up next to StackPC-PCI module, then ISA bus connector may interfere with “Connector A” of StackPC module. It also blocks using other StackPC modules above PCI-to-ISA bridge module.

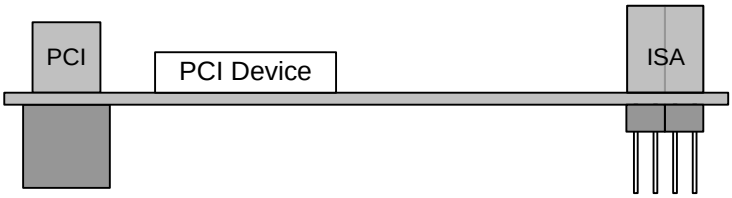


Figure 8-17: Basic configuration of the PCI-to-ISA Bridge module (PC/104-*Plus*)

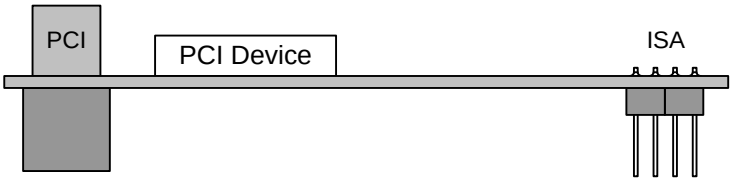


Figure 8-18: Stack-Down configuration of the PCI-to-ISA Bridge module

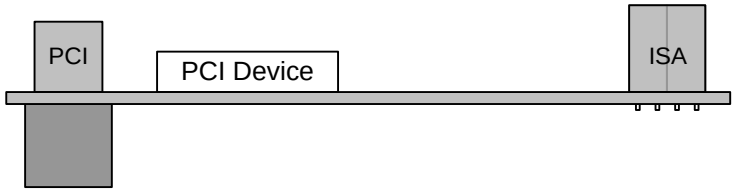


Figure 8-19: Stack-Up configuration of the PCI-to-ISA Bridge module

To allow PC/104 modules in stack it is recommended to have Basic or Stack-Down versions of a PCI-to-ISA bridge module attached to the bottom side of StackPC Host (Figure 8-20).

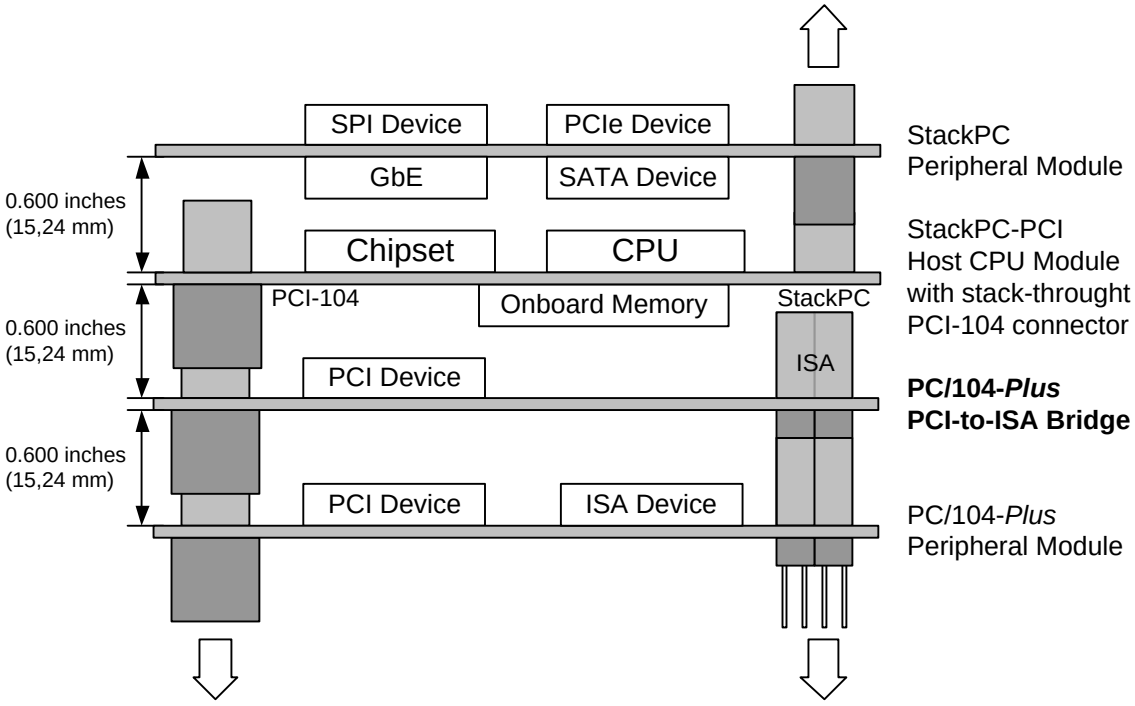


Figure 8-20: Using Basic version of PCI-to-ISA Bridge module with StackPC-PCI Host

B.2 PCI-104 (PCI)

StackPC-PCI directly supports PCI-104 since Connector B is identical to what is defined in PCI-104 and PC/104-Plus standards.

B.3 PCIe/104

StackPC and PCIe/104 form factors are mechanically identical and have several levels of compatibility depending from the set of used interfaces.

PCIe/104 specification allows Type 1 and Type 2 sets of interfaces with Type 1 having additional modes of operation with different subsets of interfaces. To allow detecting different Types of modules in stack and to avoid damaging modules PCIe/104 standard defines “stacking bits” (STK0, STK1, STK2 pins). Figure 8-21 shows how stacking bits are used by different peripheral and CPU modules. It also shows how StackPC modules should use these bits to be compatible with PCIe/104 products. If stack has modules with conflicting interfaces then Bus Stacking Error happens during system Start Up.

StackPC CPU modules shall not drive Ethernet, SATA, LPC, USB(2:5), SPI, FBUS signals until it determines that there is not a Bus Stacking Error. If the system detects a Bus Stacking Error it must remain in reset and not drive these signals. Peripheral modules shall not drive these signals while PE_RST# is asserted.

Due to “Stack-up only” concept StackPC peripheral modules can be attached only on Top of PCIe/104 Type 1 or Type 2 Host.

Bus Stacking Error formula doesn’t cover PCIe/104 Type 1 SDVO peripheral modules. Dual channel SDVO peripheral module may be damaged in case of wrong installation with Full Featured StackPC Host having Ethernet interfaces. Since new chipsets moves away from SDVO technology it is unlikely that such modules will ever appear–on the market. (Moved to Section B3 from Section B.3.4. Common problem)

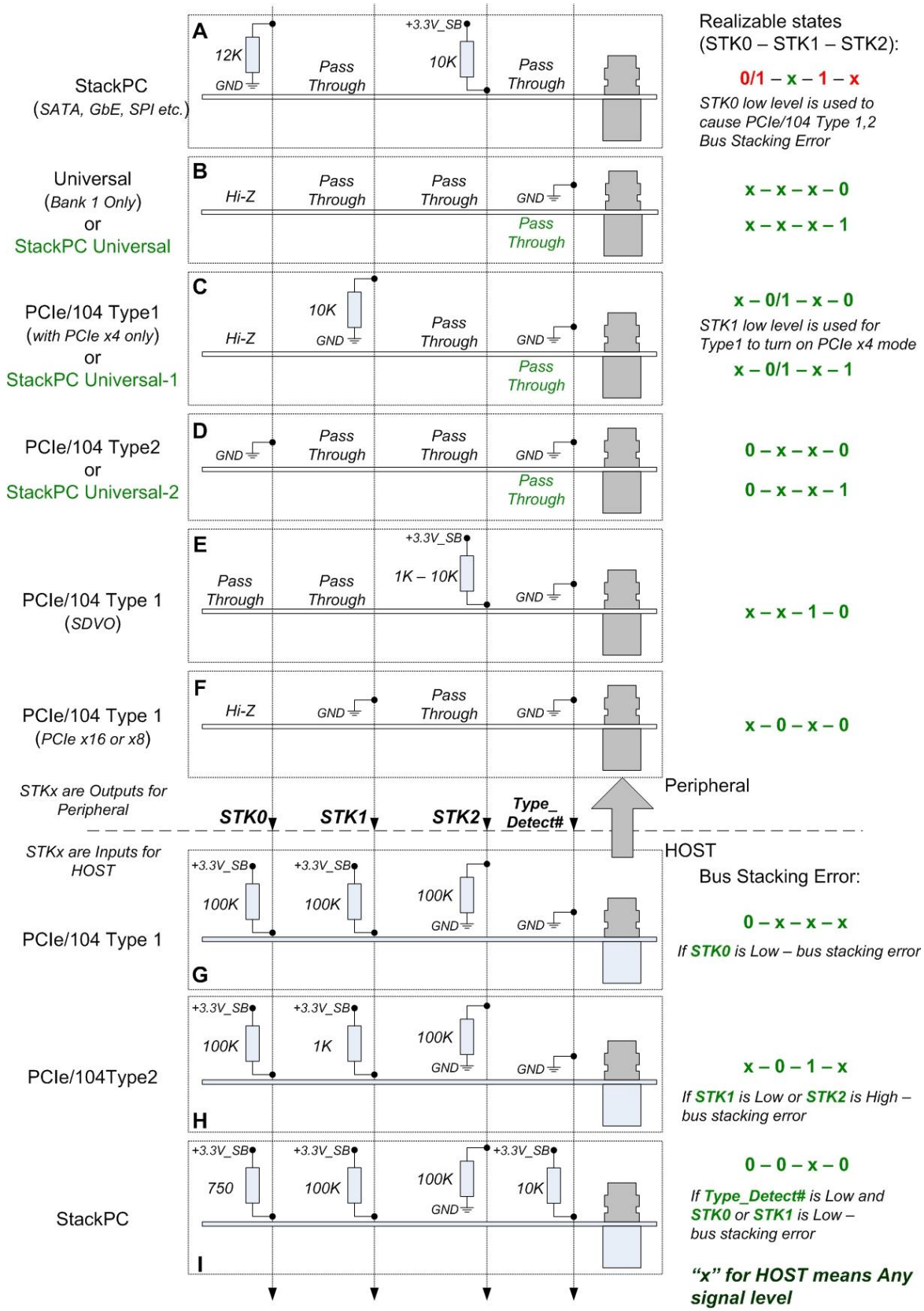


Figure 8-21: STK protection mechanism for StackPC and PCIe/104 Type 1 and Type 2 modules.

Next scheme could be used as for the reference.

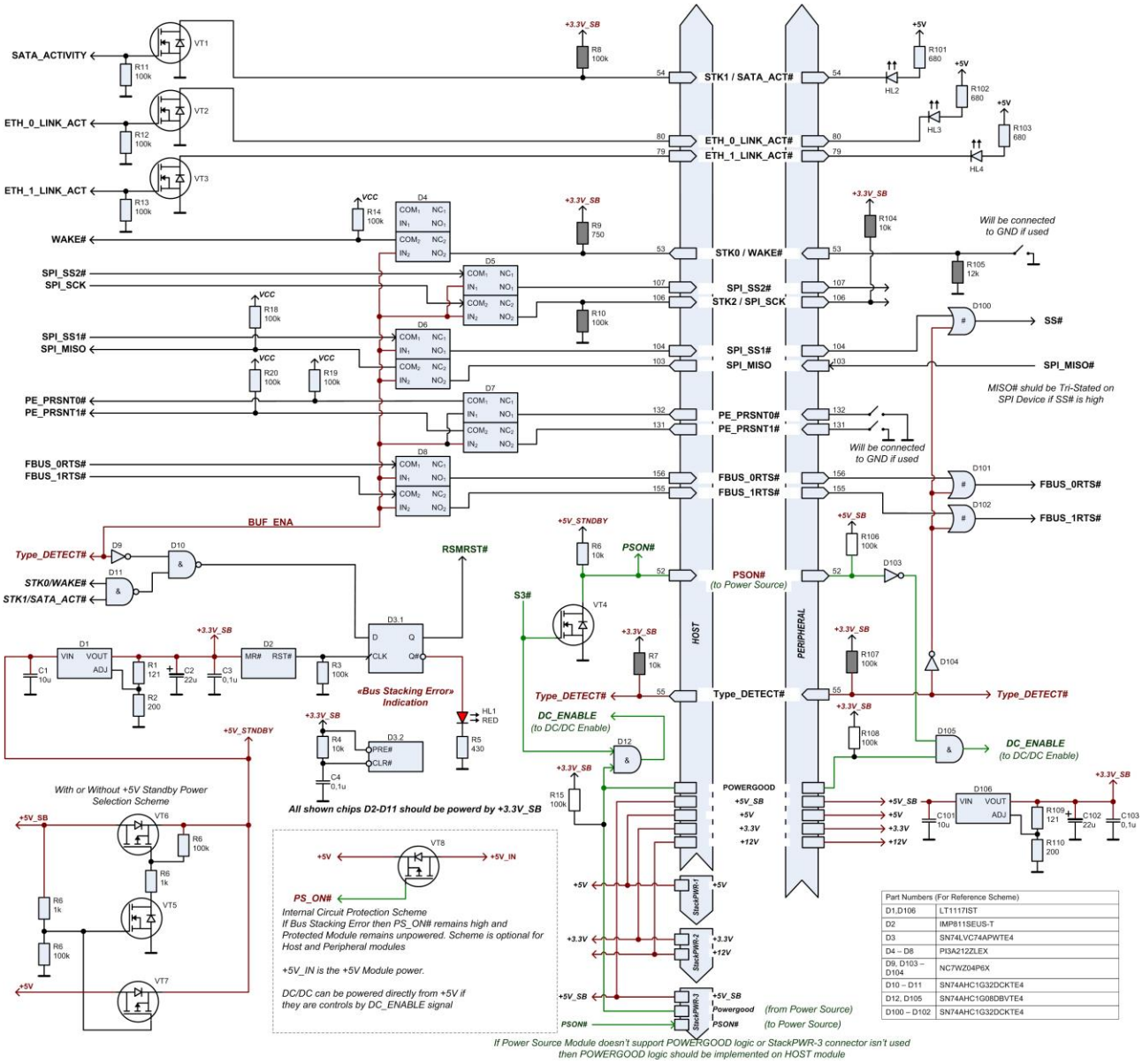


Figure 8-22: Reference schematic for StackPC modules with STK protection mechanism.

B.3.1 StackPC Universal

Table 8-5 shows subset of StackPC (Connector A) interfaces which is defined as StackPC Universal. This subset and its pin out are identical to PCIe/104 Type 1 and Type 2 Unversal pin out.

StackPC Universal peripheral modules (modules having all or part of interfaces shown in Table 8-5) are fully compatible with any PCIe/104 Type 1 or Type 2 Host.

PCIe/104 Universal peripheral modules are fully compatible with StackPC Universal Host.

Stacking bits configuration for StackPC Universal peripheral modules is shown on Figure 8-21 B.

Stacking bits configuration for StackPC Universal Host modules is shown on Figure Figure 8-21 I.

Possible Interfaces conflicts between StackPC and PCIe/104 modules:

1. No conflicts.

Table 8-5: Universal Connector A Pin Assignments

Universal Assignment, Top View (Connector A)

	1	USB_OC#	PE_RST#	2		
	3	3.3V	3.3V	4		
	5	USB_1p	USB_0p	6		
	7	USB_1n	USB_0n	8		
	9	GND	GND	10		
	11	PEx1_1Tp	PEx1_0Tp	12		
	13	PEx1_1Tn	PEx1_0Tn	14		
	15	GND	GND	16		
	17	PEx1_2Tp	PEx1_3Tp	18		
	19	PEx1_2Tn	PEx1_3Tn	20		
	21	GND	GND	22		
	23	PEx1_1Rp	PEx1_0Rp	24		
	25	PEx1_1Rn	PEx1_0Rn	26		
	27	GND	GND	28	+5 Volts	
	29	PEx1_2Rp	PEx1_3Rp	30		
	31	PEx1_2Rn	PEx1_3Rn	32		
	33	GND	GND	34		
	35	PEx1_1Clkp	PEx1_0Clkp	36		
	37	PEx1_1Clkn	PEx1_0Clkn	38		
	39	+5V_SB	+5V_SB	40		
	41	PEx1_2Clkp	PEx1_3Clkp	42		
	43	PEx1_2Clkn	PEx1_3Clkn	44		
	45	DIR	PWRGOOD	46		
	47	SMB_DAT		48		
	49	SMB_CLK		50		
	51	SMB_ALERT#	PSON#	52		BANK 1
	53	WAKE#		54		
	55		GND	56		
	57			58		
	59			60		
	61	GND	GND	62		
	63			64		
	65			66		
	67	GND	GND	68		
	69			70		
	71			72		
	73	GND	GND	74		
	75			76		
	77			78		
	79	GND	GND	80	+5 Volts	
	81			82		
	83			84		
	85	GND	GND	86		
	87			88		
	89			90		
	91	GND	GND	92		
	93			94		
	95			96		
	97	GND	GND	98		
	99			100		
	101			102		
	103		GND	104		BANK 2
	105			106		
	107	GND	GND	108		
	109			110		
	111			112		
	113	GND	GND	114		
	115			116		
	117			118		
	119	GND	GND	120		
	121			122		
	123			124		
	125	GND	GND	126		
	127			128		
	129			130		
	131	GND	GND	132	+12 Volts	
	133			134		
	135			136		
	137	GND	GND	138		
	139			140		
	141			142		
	143	GND	GND	144		
	145			146		
	147			148		
	149	GND	GND	150		
	151			152		
	153			154		
	155	GND	GND	156		BANK 3

Toward edge of board / Toward center of board

Universal Assignment, Bottom View (Connector A)

	2	PE_RST#	USB_OC#	1		
	4	3.3V	3.3V	3		
	6	USB_0p	USB_1p	5		
	8	USB_0n	USB_1n	7		
	10	GND	GND	9		
	12	PEx1_0Tp	PEx1_1Tp	11		
	14	PEx1_0Tn	PEx1_1Tn	13		
	16	GND	GND	15		
	18	PEx1_3Tp	PEx1_2Tp	17		
	20	PEx1_3Tn	PEx1_2Tn	19		
	22	GND	GND	21		
	24	PEx1_0Rp	PEx1_1Rp	23		
	26	PEx1_0Rn	PEx1_1Rn	25		
	28	GND	GND	27	+5 Volts	
	30	PEx1_3Rp	PEx1_2Rp	29		
	32	PEx1_3Rn	PEx1_2Rn	31		
	34	GND	GND	33		
	36	PEx1_0Clkp	PEx1_1Clkp	35		
	38	PEx1_0Clkn	PEx1_1Clkn	37		
	40	+5V_SB	+5V_SB	39		
	42	PEx1_3Clkp	PEx1_2Clkp	41		
	44	PEx1_3Clkn	PEx1_2Clkn	43		
	46	PWRGOOD	DIR	45		
	48		SMB_DAT	47		
	50		SMB_CLK	49		
	52	PSON#	SMB_ALERT#	51		BANK 1
	54		WAKE#	53		
	56	GND		55		
	58			57		
	60			59		
	62	GND	GND	61		
	64			63		
	66			65		
	68	GND	GND	67		
	70			69		
	72			71		
	74	GND	GND	73		
	76			75		
	78			77		
	80	GND	GND	79	+5 Volts	
	82			81		
	84			83		
	86	GND	GND	85		
	88			87		
	90			89		
	92	GND	GND	91		
	94			93		
	96			95		
	98	GND	GND	97		
	100			99		
	102			101		
	104	GND		103		BANK 2
	106			105		
	108	GND	GND	107		
	110			109		
	112			111		
	114	GND	GND	113		
	116			115		
	118			117		
	120	GND	GND	119		
	122			121		
	124			123		
	126	GND	GND	125		
	128			127		
	130			129		
	132	GND	GND	131	+12 Volts	
	134			133		
	136			135		
	138	GND	GND	137		
	140			139		
	142			141		
	144	GND	GND	143		
	146			145		
	148			147		
	150	GND	GND	149		
	152			151		
	154			153		
	156	GND	GND	155		BANK 3

Toward center of board / Toward edge of board

USB Interface
PCI-Express Interface
ATX Power Supply
SMBus Interface
Power Interface
Pass Through

GND
Connected to GND plane both on Host and Peripheral modules.

GND
Connected to GND plane on Host, Pass Through on peripheral modules.

B.3.2 StackPC Universal-1

Table 8-6 shows subset of StackPC (Connector A) interfaces which is defined as StackPC Universal-1. This subset and its pin out is identical to PCIe/104 Type 1 (x4 PCIe) and Type 2 pin outs. StackPC Universal-1 subset has interfaces of StackPC Universal subset plus 1x4 PCIe link.

StackPC Universal-1 peripheral modules are compatible with PCIe/104 Type 1 (x4 PCIe) and Type 2 Hosts.

PCIe/104 peripheral modules with Universal-1 interfaces are fully compatible with StackPC Universal-1 Hosts.

StackPC Universal-1 peripheral modules can be freely used in PCIe/104 systems with 2 x4 PCIe links. If such system has a mix of StackPC and PCIe/104 peripheral modules each using x4 PCIe link, then PCIe/104 peripheral module should be first to Host module.

Stacking bits configuration for StackPC Universal-1 peripheral modules is shown on Figure 8-21 C.

Stacking bits configuration for StackPC Universal-1 Host modules is shown on Figure 8-21 I.

Possible Interfaces conflicts between StackPC and PCIe/104 modules:

1. No conflicts.

StackPC peripheral module using x4 PCI-E should be next to PCIe/104 peripheral module using the first x4 PCI-E link. StackPC peripheral module doesn’t implement link shifting for x4 PCI-E links

Table 8-6: Universal-1 Connector A Pin Assignments

Universal-1, Assignment, Top View (Connector A)

	1	USB_OC#	PE_RST#	2			
	3	3.3V	3.3V	4			
	5	USB_5p	USB_4p	6			
	7	USB_5n	USB_4n	8			
	9	GND	GND	10			
	11	PEx1_1Tp	PEx1_0Tp	12			
	13	PEx1_1Tn	PEx1_0Tn	14			
	15	GND	GND	16			
	17	PEx1_2Tp	PEx1_3Tp	18			
	19	PEx1_2Tn	PEx1_3Tn	20			
	21	GND	GND	22			
	23	PEx1_1Rp	PEx1_0Rp	24			
	25	PEx1_1Rn	PEx1_0Rn	26			
	27	GND	GND	28			
	29	PEx1_2Rp	PEx1_3Rp	30			
	31	PEx1_2Rn	PEx1_3Rn	32			
	33	GND	GND	34			
	35	PEx1_1Clkp	PEx1_0Clkp	36			
	37	PEx1_1Clkn	PEx1_0Clkn	38			
	39	+5V_SB	+5V_SB	40			
	41	PEx1_2Clkp	PEx1_3Clkp	42			
	43	PEx1_2Clkn	PEx1_3Clkn	44			
	45	DIR	PWRGOOD	46			
	47	SMB_DAT	PE_x4_CLKp	48			
	49	SMB_CLK	PE_x4_CLKn	50			
	51	SMB_ALERT#	PSON#	52			
	53	STK0 / WAKE#	STK1 / PEG_ENA#	54			
	55		GND	56			
	57		PEx4_0T(0)p	58			
	59		PEx4_0T(0)n	60			
	61	GND	GND	62			
	63		PEx4_0T(1)p	64			
	65		PEx4_0T(1)n	66			
	67	GND	GND	68			
	69		PEx4_0T(2)p	70			
	71		PEx4_0T(2)n	72			
	73	GND	GND	74			
	75		PEx4_0T(3)p	76			
	77		PEx4_0T(3)n	78			
	79	GND	GND	80			
	81			82			
	83			84			
	85	GND	GND	86			
	87			88			
	89			90			
	91	GND	GND	92			
	93			94			
	95			96			
	97	GND	GND	98			
	99			100			
	101			102			
	103		GND	104			
	105	STK2		106			
	107	GND	GND	108			
	109		PEx4_0R(0)p	110			
	111		PEx4_0R(0)n	112			
	113	GND	GND	114			
	115		PEx4_0R(1)p	116			
	117		PEx4_0R(1)n	118			
	119	GND	GND	120			
	121		PEx4_0R(2)p	122			
	123		PEx4_0R(2)n	124			
	125	GND	GND	126			
	127		PEx4_0R(3)p	128			
	129		PEx4_0R(3)n	130			
	131	GND	GND	132			
	133			134			
	135			136			
	137	GND	GND	138			
	139			140			
	141			142			
	143	GND	GND	144			
	145			146			
	147			148			
	149	GND	GND	150			
	151			152			
	153			154			
	155	GND	GND	156			

Toward edge of board / Toward center of board / +5 Volts / +12 Volts / BANK 1 / BANK 2 / BANK 3

Universal-1, Assignment, Bottom View (Connector A)

	2	PE_RST#	USB_OC#	1			
	4	3.3V	3.3V	3			
	6	USB_4p	USB_5p	5			
	8	USB_4n	USB_5n	7			
	10	GND	GND	9			
	12	PEx1_0Tp	PEx1_1Tp	11			
	14	PEx1_0Tn	PEx1_1Tn	13			
	16	GND	GND	15			
	18	PEx1_3Tp	PEx1_2Tp	17			
	20	PEx1_3Tn	PEx1_2Tn	19			
	22	GND	GND	21			
	24	PEx1_0Rp	PEx1_1Rp	23			
	26	PEx1_0Rn	PEx1_1Rn	25			
	28	GND	GND	27			
	30	PEx1_3Rp	PEx1_2Rp	29			
	32	PEx1_3Rn	PEx1_2Rn	31			
	34	GND	GND	33			
	36	PEx1_0Clkp	PEx1_1Clkp	35			
	38	PEx1_0Clkn	PEx1_1Clkn	37			
	40	+5V_SB	+5V_SB	39			
	42	PEx1_3Clkp	PEx1_2Clkp	41			
	44	PEx1_3Clkn	PEx1_2Clkn	43			
	46	PWRGOOD	DIR	45			
	48	PE_x4_CLKp	SMB_DAT	47			
	50	PE_x4_CLKn	SMB_CLK	49			
	52	PSON#	SMB_ALERT#	51			
	54	STK1 / PEG_ENA#	STK0 / WAKE#	53			
	56	GND		55			
	58	PEx4_0T(0)p		57			
	60	PEx4_0T(0)n		59			
	62	GND	GND	61			
	64	PEx4_0T(1)p		63			
	66	PEx4_0T(1)n		65			
	68	GND	GND	67			
	70	PEx4_0T(2)p		69			
	72	PEx4_0T(2)n		71			
	74	GND	GND	73			
	76	PEx4_0T(3)p		75			
	78	PEx4_0T(3)n		77			
	80	GND	GND	79			
	82			81			
	84			83			
	86	GND	GND	85			
	88			87			
	90			89			
	92	GND	GND	91			
	94			93			
	96			95			
	98	GND	GND	97			
	100			99			
	102			101			
	104	GND		103			
	106		STK2	105			
	108	GND	GND	107			
	110	PEx4_0R(0)p		109			
	112	PEx4_0R(0)n		111			
	114	GND	GND	113			
	116	PEx4_0R(1)p		115			
	118	PEx4_0R(1)n		117			
	120	GND	GND	119			
	122	PEx4_0R(2)p		121			
	124	PEx4_0R(2)n		123			
	126	GND	GND	125			
	128	PEx4_0R(3)p		127			
	130	PEx4_0R(3)n		129			
	132	GND	GND	131			
	134			133			
	136			135			
	138	GND	GND	137			
	140			139			
	142			141			
	144	GND	GND	143			
	146			145			
	148			147			
	150	GND	GND	149			
	152			151			
	154			153			
	156	GND	GND	155			

Toward center of board / Toward edge of board / +5 Volts / +12 Volts / BANK 2 / BANK 3

USB Interface
PCI-Express Interface
PCI-Express x4 Interface
ATX Power Supply
SMBus Interface
Power Interface
Pass Through

GND

Connected to GND plane both on Host and Peripheral modules.

GND

Connected to GND plane on Host, Pass Through on peripheral modules.

B.3.3 StackPC Universal-2

Table 8-7 shows subset of StackPC (Connector A) interfaces which is defined as StackPC Universal-2. This subset and its pin out are identical to subset of PCIe/104 Type 2 interfaces. StackPC Universal-2 subset has interfaces of StackPC Universal-1 subset plus RTC_Battery, LPC and SATA interfaces.

StackPC Universal-2 peripheral modules are compatible with PCIe/104 Type 2 Hosts.

PCIe/104 peripheral modules with Universal-2 interfaces are compatible with StackPC Universal-2 Hosts.

Stacking bits configuration for StackPC Universal-1 peripheral modules is shown on Figure 8-21 D.

Stacking bits configuration for StackPC Universal-1 Host modules is shown on Figure 8-21 H.

Possible Interfaces conflicts between StackPC and PCIe/104 modules:

1. Like PCIe/104 Type 2, StackPC Universal-2 modules have potential interfaces conflict with PCIe/104 Type 1 modules which use x8, x16 PCIe links. Conflict has to be resolved the same way as it is defined in PCIe/104 specification – using staking bits to detect Bus Stacking Error situation.

Bus Stacking Error is detected during Start Up if “(STK0=0 Or STK1=0) And Type_DETECT# = 0”. This condition becomes TRUE if Type 1 peripheral module using PCIe link wider than x4 is plugged to StackPC Universal-2 Host. In such case system should stay in Reset state and StackPC Universal-2 modules should not drive SATA and LPC signals on the bus.

Table 8-7: Universal-2 Connector A Pin Assignments

Universal-2, Assignment, Top View (Connector A)						**Universal-2**, Assignment, Bottom View (Connector A)					
	1	USB_OC#	PE_RST#	2			2	PE_RST#	USB_OC#	1	
	3	3.3V	3.3V	4			4	3.3V	3.3V	3	
	5	USB_5p	USB_4p	6			6	USB_4p	USB_5p	5	
	7	USB_5n	USB_4n	8			8	USB_4n	USB_5n	7	
	9	GND	GND	10			10	GND	GND	9	
	11	PEx1_1Tp	PEx1_0Tp	12			12	PEx1_0Tp	PEx1_1Tp	11	
	13	PEx1_1Tn	PEx1_0Tn	14			14	PEx1_0Tn	PEx1_1Tn	13	
	15	GND	GND	16			16	GND	GND	15	
	17	PEx1_2Tp	PEx1_3Tp	18			18	PEx1_3Tp	PEx1_2Tp	17	
	19	PEx1_2Tn	PEx1_3Tn	20			20	PEx1_3Tn	PEx1_2Tn	19	
	21	GND	GND	22			22	GND	GND	21	
	23	PEx1_1Rp	PEx1_0Rp	24			24	PEx1_0Rp	PEx1_1Rp	23	
	25	PEx1_1Rn	PEx1_0Rn	26	+5 Volts	BANK 1	26	PEx1_0Rn	PEx1_1Rn	25	+5 Volts
	27	GND	GND	28			28	GND	GND	27	
	29	PEx1_2Rp	PEx1_3Rp	30			30	PEx1_3Rp	PEx1_2Rp	29	
	31	PEx1_2Rn	PEx1_3Rn	32			32	PEx1_3Rn	PEx1_2Rn	31	
	33	GND	GND	34			34	GND	GND	33	
	35	PEx1_1Clkp	PEx1_0Clkp	36			36	PEx1_0Clkp	PEx1_1Clkp	35	
	37	PEx1_1Clkn	PEx1_0Clkn	38			38	PEx1_0Clkn	PEx1_1Clkn	37	
	39	+5V_SB	+5V_SB	40			40	+5V_SB	+5V_SB	39	
	41	PEx1_2Clkp	PEx1_3Clkp	42			42	PEx1_3Clkp	PEx1_2Clkp	41	
	43	PEx1_2Clkn	PEx1_3Clkn	44			44	PEx1_3Clkn	PEx1_2Clkn	43	
	45	DIR	PWRGOOD	46			46	PWRGOOD	DIR	45	
	47	SMB_DAT	PE_x4_CLKp	48			48	PE_x4_CLKp	SMB_DAT	47	
	49	SMB_CLK	PE_x4_CLKn	50			50	PE_x4_CLKn	SMB_CLK	49	
	51	SMB_ALERT#	PSON#	52			52	PSON#	SMB_ALERT#	51	
Toward edge of board	53	STK0 / WAKE#	STK1 / SATA_ACT#	54			54	STK1 / SATA_ACT#	STK0 / WAKE#	53	Toward edge of board
	55		GND	56			56	GND		55	
	57		PEx4_0T(0)p	58			58	PEx4_0T(0)p		57	
	59		PEx4_0T(0)n	60			60	PEx4_0T(0)n		59	
	61	GND	GND	62			62	GND	GND	61	
	63		PEx4_0T(1)p	64			64	PEx4_0T(1)p		63	
	65		PEx4_0T(1)n	66			66	PEx4_0T(1)n		65	
	67	GND	GND	68			68	GND	GND	67	
	69		PEx4_0T(2)p	70			70	PEx4_0T(2)p		69	
	71		PEx4_0T(2)n	72			72	PEx4_0T(2)n		71	
	73	GND	GND	74			74	GND	GND	73	
	75		PEx4_0T(3)p	76			76	PEx4_0T(3)p		75	
	77		PEx4_0T(3)n	78			78	PEx4_0T(3)n		77	
	79	GND	GND	80			80	GND	GND	79	
	81	SATA_T1p	SATA_T0p	82			82	SATA_T0p	SATA_T1p	81	
	83	SATA_T1n	SATA_T0n	84			84	SATA_T0n	SATA_T1n	83	
	85	GND	GND	86	+5 Volts	BANK 2	86	GND	GND	85	+5 Volts
	87			88			88			87	
	89			90			90			89	
	91	GND	GND	92			92	GND	GND	91	
	93			94			94			93	
	95			96			96			95	
	97	GND	GND	98			98	GND	GND	97	
	99			100			100			99	
	101			102			102			101	
Toward center of board	103		GND	104			104	GND		103	Toward center of board
	105	STK2	LPC_CLK	106			106	LPC_CLK	STK2	105	
	107	GND	GND	108			108	GND	GND	107	
	109		PEx4_0R(0)p	110			110	PEx4_0R(0)p		109	
	111		PEx4_0R(0)n	112			112	PEx4_0R(0)n		111	
	113	GND	GND	114			114	GND	GND	113	
	115		PEx4_0R(1)p	116			116	PEx4_0R(1)p		115	
	117		PEx4_0R(1)n	118			118	PEx4_0R(1)n		117	
	119	GND	GND	120			120	GND	GND	119	
	121		PEx4_0R(2)p	122			122	PEx4_0R(2)p		121	
	123		PEx4_0R(2)n	124			124	PEx4_0R(2)n		123	
	125	GND	GND	126			126	GND	GND	125	
	127		PEx4_0R(3)p	128			128	PEx4_0R(3)p		127	
	129		PEx4_0R(3)n	130			130	PEx4_0R(3)n		129	
	131	GND	GND	132	+12 Volts	BANK 3	132	GND	GND	131	+12 Volts
	133	SATA_R1p	SATA_R0p	134			134	SATA_R0p	SATA_R1p	133	
	135	SATA_R1n	SATA_R0n	136			136	SATA_R0n	SATA_R1n	135	
	137	GND	GND	138			138	GND	GND	137	
	139			140			140			139	
	141			142			142			141	
	143	GND	GND	144			144	GND	GND	143	
	145	LPC_AD0	LPC_DRQ#	146			146	LPC_DRQ#	LPC_AD0	145	
	147	LPC_AD1	LPC_SERIRQ#	148			148	LPC_SERIRQ#	LPC_AD1	147	
	149	GND	GND	150			150	GND	GND	149	
	151	LPC_AD2	LPC_FRAME#	152			152	LPC_FRAME#	LPC_AD2	151	
	153	LPC_AD3	*RTC_Battery*	154			154	*RTC_Battery*	LPC_AD3	153	
	155	GND	GND	156			156	GND	GND	155	

USB Interface
PCI-Express Interface
PCI-Express x4 Interface
SATA Interface
ATX Power Supply
SMBus Interface
Power Interface
Pass Through

GND
Connected to GND plane both on Host and Peripheral modules.

GND
Connected to GND plane on Host, Pass Through on peripheral modules.

B.3.4 Full Featured StackPC

Table 2-1 shows complete set of StackPC (Connector A) interfaces. Complete set of StackPC interfaces has interfaces of StackPC Universal-2 subset plus 2x Ethernet, 3x SPI, 2x Express Card, and additional 4 ports of USB 2.0 interfaces.

Stacking bits configuration for full featured StackPC peripheral modules is shown on Figure 8-21 A.

Stacking bits configuration for full featured StackPC Host modules is shown on Figure 8-21 I.

Possible Interfaces conflicts between StackPC and PCIe/104 modules:

1. Full Featured StackPC Host module has potential interfaces conflict with PCIe/104 Type 1 and Type 2 modules using Bank 2 and Bank 3 signals on Connector A. Since current PCIe/104 specification doesn't allow Host to understand what particular set of interfaces is used by PCIe/104 peripherals, then Full Featured StackPC Host should consider presence of any PCIe/104 Type 1 or Type 2 module other than Universal as a Bus Stacking Error. StackPC Host uses Type_DETECT# signal to define that PCIe/104 Type 1 or Type 2 modules are presented and uses stacking bits to define that there is at least one not Universal module among them.

Bus Stacking Error is detected during Start Up if "(STK0=0 Or STK1=0) And Type_DETECT#=0". In such case system should stay in Reset state and Full Featured StackPC modules should not drive SATA, LPC, Ethernet, SPI, USB(2:5) signals on the bus (Figure 8-23).

According above rules Full Featured StackPC modules can work with any PCIe/104 Universal modules in one stack. Implementing recommendations described below in subsection B.3.5 allows improving compatibility between Full Featured StackPC modules and PCIe/104 modules from Universal to Universal-2 set of interfaces.

2. Full featured StackPC modules may use several pins that are grounded according PCIe/104 specification. Type_DETECT# signal (pin 55) is pulled-up on Host and is used to detect presence of PCIe/104 modules in mixed stack, so grounding this pin by PCIe/104 peripheral module is normal situation. Below is the list of StackPC pins that are effected by ground pins of PCIe/104 modules in mixed stack.

    - Ethernet Indication Eth_LINK_ACT# (pins 79, 80)
    - SPI Bus (pins 103, 104, 107)
    - ExpressCard detection PE_PRSNT# (pins 131, 132)
    - FBUS drivers control lines FBUS_RTS# (pins 155, 156)

If Full Featured StackPC Host is mixed with PCIe/104 peripheral then SPI bus, FBUS_RTS#, PE_PRSNT#, and ETH_LINK_ACT# lines become unavailable. It doesn't effect other StackPC interfaces including data links for Ethernet and FBUS which remains available.

To avoid damages because of mixing Full Featured StackPC and PCIe/104 modules in one stack, outputs for that signals should be Open Drain or should be switched to High-Z state in case Type_DETECT# is Low (Figure 8-23). Buffers are shown as an example. It is up to designer to choose particular implementation of safety measures. PE_PRSNT# signals may not require output buffer since they pulled-up on Host and left unconnected or grounded on ExpressCard module. Input buffers for SPI_SS, FBUS_RTS signals may also not be necessary.

Implementing recommendations described below in subsection B.3.5 allows using all signals mentioned above in mixed stack.

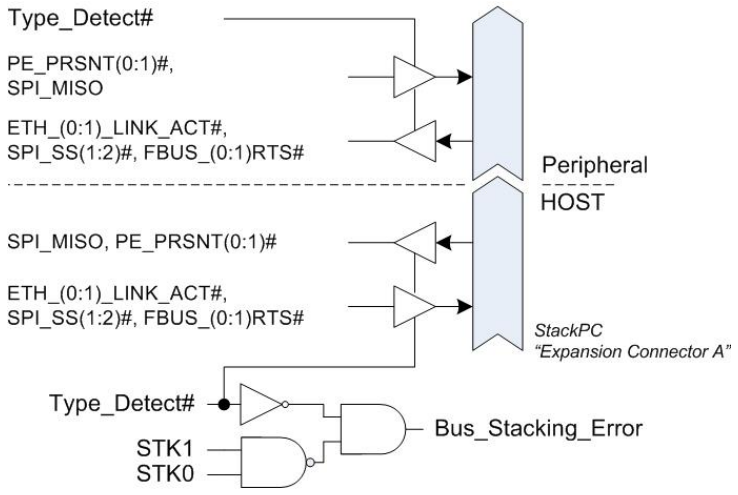


Figure 8-23: Bus Stacking Error and Type_DETECT# logic for full featured StackPC Host and peripherals

B.3.5 PCIe/104 design recommendations to support StackPC modules

There are two recommendations which can be used for new PCIe/104 modules designs or for modifying existing designs to improve StackPC and PCIe/104 modules compatibility in mixed stack.

1. It is recommended that PCIe/104 modules connect Type_DETECT# pin (Connector A pin 55) to the GND only in case they use interfaces that are in conflict with StackPC specific interfaces. It means that PCIe/104 Type 1 or Type 2 Host and Peripheral modules should have that pin unconnected (for Host) or pass through (for peripherals) if they use interfaces within StackPC Universal-2 set of interfaces. PCIe/104 modules should ground Type_DETECT# pin only if modules use interfaces (pins) outside StackPC Universal-2 pin out. PCIe/104 modules which

shifts second x4 PCIe link are considered as using second x4 PCIe link, so such modules should ground Type_DETECT# pin, since second x4 PCIe link is outside Universal-2 pin out.

Bus Stacking Error logic for StackPC modules stays the same while compatibility of StackPC and PCIe/104 modules in mixed stack is improved from Universal to Universal-2 set of interfaces.

2. It is recommended that for PCIe/104 peripheral modules using pins within StackPC Universal-2 pin out, pins numbered 79, 80, 103, 104, 107, 131, 132, 155, and 156 to be converted from ground to pass through. Thus in case of mixed stack PCIe/104 peripherals will not effect availability of ETH_LINK_ACT#, SPI, PE_PRSNT#, and FBUS_RTS# signals for Full Featured StackPC peripheral modules.

Following both of these recommendations allows using Full Featured StackPC Host and peripheral modules in mix with any PCIe/104 modules using interfaces within Universal-2 set of interfaces. In addition Express Cards support becomes possible for StackPC Host having any combination of interfaces (Universal, Universal-1, Universal-2, and Full Featured)

3. According to PCIe/104 specification, systems using Type 2 peripheral modules do not support WAKE# signal. STK0/WAKE# signal on Type 2 peripheral modules is always connected to the GND to generate Bus Stacking Error if Type 1 Host and Type 2 peripheral modules are mixed in the same stack. For compatibility reason StackPC Universal-2 peripheral modules also have that pin connected to the GND. To make WAKE# signal possible in systems using PCIe/104 Type 2 or StackPC Universal-2 peripheral modules it is recommended for such modules to allow end user to disconnect STK0/WAKE# pins from GND plane after end user makes sure that Type 1 Host is not used in the system.

B.3.6 Interfaces compatibility summary

Table 8-8 shows compatibility matrix for various PCIe/104 and StackPC pin outs.

Table 8-8: StackPC and PCIe/104 Compatibility table

Interface	Module Type					
	Type1	Type2	StackPC	Universal	Universal-1	Universal-2
Bank1 Interfaces (4xPCIe,2xUSB,SMB)	V	V	V	V	V	V
1 x16 PCI-Express	V	X	X	PASS	PASS	X
2 SDVO	V	X	X	PASS	PASS	X
2 x8 PCI-Express	V	X	X	PASS	PASS	X
1st x4 PCI-Express	V	V	V	PASS	V	V
2nd x4 PCI-Express	V	V	X	PASS	PASS	PASS
2x PE_PRSNT0#	PASS	PASS	V	PASS	PASS	PASS
2x SATA (Data Lines)	X	V	V	PASS	PASS	V
2x SATA (Control Lines)	X	V	X	PASS	PASS	PASS
LPC	X	V	V	PASS	PASS	V
2x USB 3.0	X	V	X	PASS	PASS	PASS
4x USB 2.0 (USB2..5)	X	X	V	PASS	PASS	PASS
2x GbE	X	X	V	PASS	PASS	PASS
2x FBUS (Rx/Tx)	X	X	V	PASS	PASS	PASS
SPI	X	X	V	PASS	PASS	PASS
RTC_Battery	X	V	V	PASS	PASS	V

V	Interface can be Implemented by module and can be used in stack
PASS	Interface can be used by other modules when such module is installed in the same stack
X	Interface can't be used by other modules when such module is installed in the same stack (Bus Stacking Error)

StackPC Universal and StackPC Universal-1 modules are fully compatible with PCIe/104 modules supporting 4 x 1 PCIe, 1 x 4 PCIe, USB(0:1), and SMB. There are no interface conflicts.

StackPC Universal-2 modules are fully compatible with PCIe/104 Type 2 modules supporting 4 x 1 PCIe, 1 x 4 PCIe, USB(0:1), SATA(0:1) (data links), LPC, RTC_Battery and SMB. Interface conflicts are possible with PCIe/104 Type 1 modules using x8 PCIe or, x16 PCIe links. StackPC Universal-2 modules use the same way for conflict resolving as PCIe/104 Type 2 modules do.

Full featured StackPC modules are compatible with PCIe/104 Universal modules supporting 4 x 1 PCIe, USB(0:1), and SMB. Mixing full featured StackPC modules with PCIe/104 modules other than Universal causes Bus Stacking Error. Thus in stack where full featured StackPC modules are mixed with existing PCIe/104 modules only PCIe/104 Universal modules can be used. If PCIe/104 modules implement recommendations described in B.3.5, then all StackPC interfaces (4 x 1 PCIe, 1 x 4 PCIe, USB(0:5),

SATA(0:1) (data links), Ethernet(0:1), ExpressCard(0:1), FBUS(0:1), LPC, RTC_Battery and SMB) can be used by full featured StackPC modules in one stack together with any PCIe/104 Type 1 or Type 2 modules using interfaces within Universal-2 set of interfaces (4 x 1 PCIe 1 x 4 PCIe, USB(0:1), SATA(0:1) (data links), LPC, RTC_Battery and SMB).

B.3.7 Stack-Up and Stack-Down configurations

PCIe/104 specification defines Stack-Up or Stack-Down configurations. In the same time if Host interfaces on its Top and Bottom connectors are connected then only one configuration is possible: Stack-Up or Stack-Down. As a result Host module should be always the first module in stack. StackPC follows the same rule: Host module should be always the first modules in StackPC stack and can be on Top or Bottom of the stack depending from whole stack orientation. Moreover since StackPC clearly defines from what side of Host modules StackPC modules should be stacked, it simplifies system design and allows more standardized cooling solutions.

PCIe/104 specification defines that if Host module interfaces on its Top and Bottom connectors are not connected then Stack-Up and Stack-Down configuration can be used simultaneously with possibility for Host module to be in the middle of a stack. Since StackPC specification doesn't limit usage of Bottom side of Host module, then PCIe/104 Type 1 or Type 2 connectors can be located on Bottom side providing Stack-Down configuration for Type 1 or Type 2 modules (Figure 8-24).

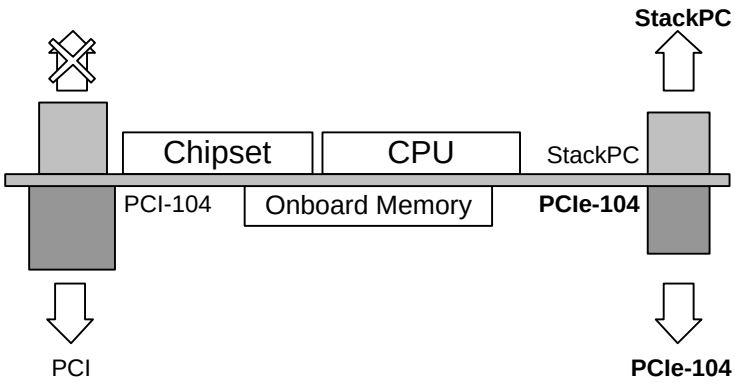


Figure 8-24: StackPC-PCI Host module with optional PCI/104-Express Support

In addition StackPC-PCI Host modules allow PCI/104 peripheral modules to be stacked up or down depending from system designer preferences or application requirements.

Providing Stack-Up configuration for StackPC modules and Stack-Down configuration for PCIe/104 (Type 1 or Type 2), StackPC is compatible with PCIe/104 specification in regards of stacking flexibility (Figure 8-25).

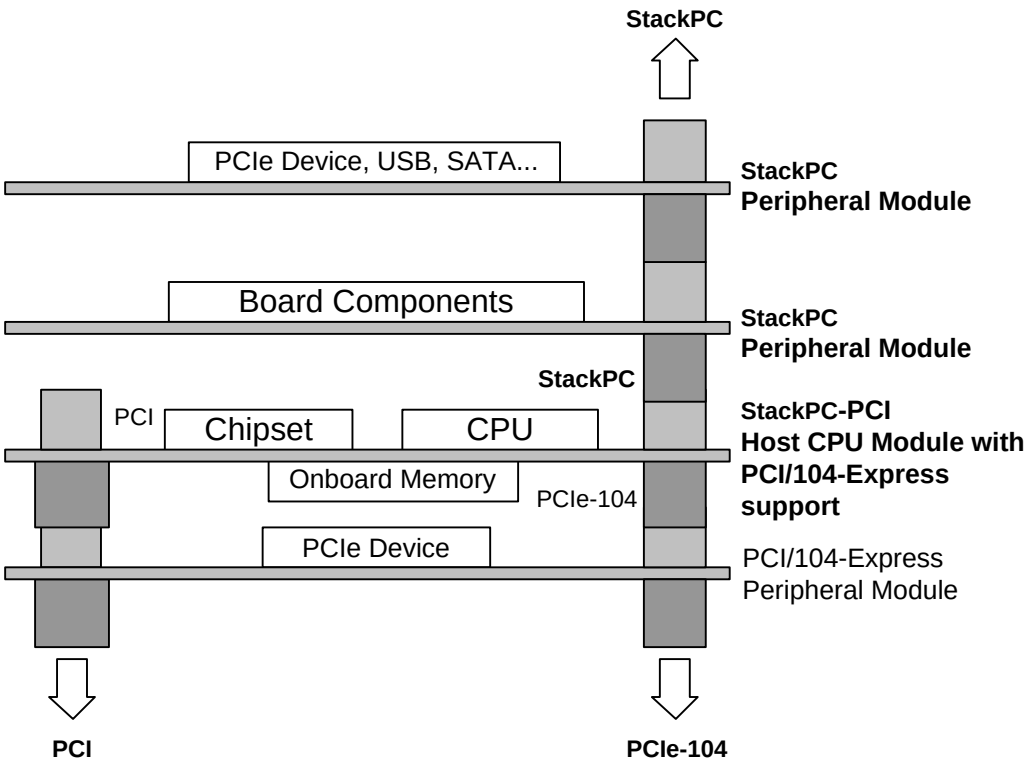


Figure 8-25: StackPC-PCI Host module with StackPC modules on Top and PCI/104-Express module on Bottom

B.3.8 x16 PCIe link support

Like PCIe/104 Type 2 StackPC does not support x16 PCIe link on Connector A. There are two ways to provide support for PCIe/104 Type 1 peripheral modules which use x16 or x8 PCIe link:

1. To use Host with PCIe/104 Type 1 connector on Bottom side (Figure 8-26).

2. To use StackPC-FPE Host in combination with StackPC-FPE to PCIe/104 Type 1 bridge (Figure 8-27).

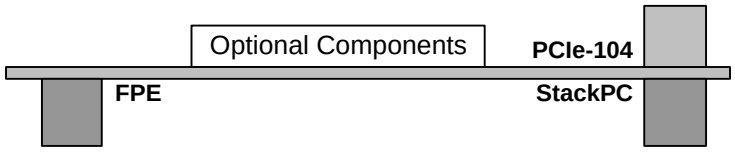


Figure 8-26: «StackPC-FPE to PCIe/104» bridge module

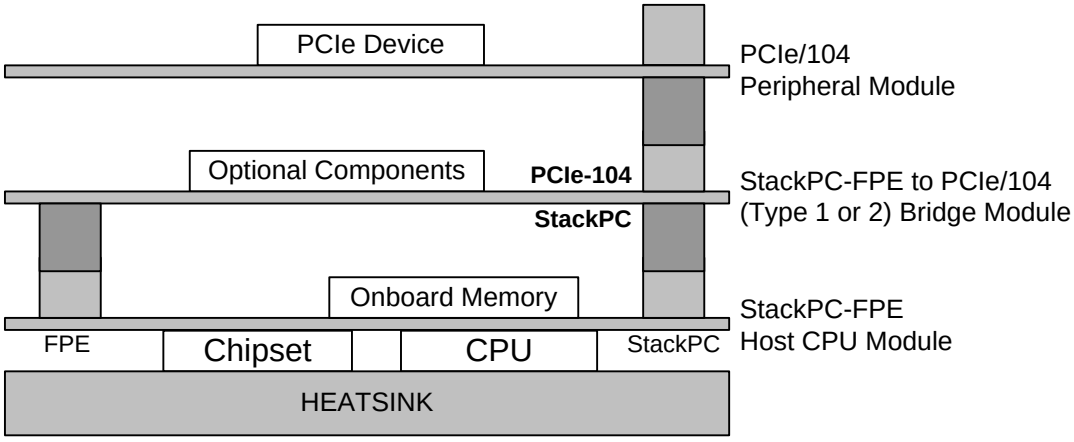


Figure 8-27: Stack using «StackPC-FPE to PCIe/104» bridge module

B.3.9 StackPC products labeling

It is recommended to indicate clearly what set of interfaces is implemented by particular StackPC module to allow end user quickly understand the level of its compatibility with StackPC and PCIe/104 modules. It is recommended to show this information in datasheets and by marking PCB nearby Connector A according following rules:

“StackPC U” – Implemented interfaces are within StackPC Universal set of interfaces.

“StackPC U1” – Implemented interfaces are within StackPC Universal-1 set of interfaces.

“StackPC U2” – Implemented interfaces are within StackPC Universal-2 set of interfaces.

“StackPC FF” – Any StackPC specific interface (outside of Universal-2 set) is implemented (i.e. GbE(0:1), USB(2:5), FBUS, or SPI). StackPC Full Featured or contains StackPC specific set of interfaces module.

It is also recommended to mark PCIe/104 modules, where B.3.5 recommendations are implemented, with “StackPC” sign.

APPENDIX C: Expansion Connector B1 (FPE) Configurable Section Profiles.

FPE Connector includes Configurable section where pin out may have up to 8 different profiles which can be recognized by state of Config_Type(0:2) signals. In general each peripheral module with FPE can pass through, and/or substitute and/or add its own signals to FPE. It includes possibility to work with one profile on Bottom FPE connector and with another profile on the Top. Thus each FPE module can be a Host for next FPE module in Stack. So Host signals and pin assignments described for different profiles below are applied to Top FPE connector of CPU or peripheral module. Depending from profile number link shifting can be used.

If StackPC-FPE peripheral module does not use Configurable Section pins neither on Bottom nor on Top connector such module should have Configurable Section transparent. It means that all Configurable Section and Config_Type(0:2) pins should be pass through.

In case Top connector Profile number is not equal to Bottom connector Profile number expected by next module in stack then next module drives FPE_Bus_Err# signal Low indicating to CPU module that Bus Stacking Error is detected.

C.1 FPE Profile-7 (Unused)

Host: Config_Type(0:2) = 111 (“1” - 10K Pull-up)

This Host profile indicates to the next StackPC-FPE module in stack that Configurable Section is not used. Host lefts unconnected all Configurable Section pins on its Top FPE connector.

Table 8-9: Connector B1 (FPE) Profile-7 Pin assignments

Top View Profile-7 Signals Assignment of Connector B1 (FPE)											
		ROWS									
		10	9	8	7	6	5	4	3	2	1
COLUMNS (EDGE OF THE BOARD)	1	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	AUX_CH+	HOT_PLUG
	2	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	AUX_CH-	GND
	3	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	DP_PWR	ML_L(1)p
	4	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	ML_L(3)p	ML_L(1)n
	5	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	ML_L(3)n	GND
	6	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	GND	ML_L(0)p
	7	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	Unconnected	ML_L(2)p	ML_L(0)n
	8	Unconnected	Unconnected	Unconnected	GND	Unconnected	GND	Unconnected	GND	ML_L(2)n	GND
	9	Reserved	Reserved	GND	PEx16_0T(6)p	GND	PEx16_0T(4)p	GND	PEx16_0T(2)p	GND	PEx16_0T(0)p
	10	Reserved	Reserved	PEx16_0T(7)p	PEx16_0T(6)n	PEx16_0T(5)p	PEx16_0T(4)n	PEx16_0T(3)p	PEx16_0T(2)n	PEx16_0T(1)p	PEx16_0T(0)n
	11	PE_RST#	GND	PEx16_0T(7)n	GND	PEx16_0T(5)n	GND	PEx16_0T(3)n	GND	PEx16_0T(1)n	GND
	12	GND	PEx16_x8_x4_0Clkp	GND	PEx16_0R(6)p	GND	PEx16_0R(4)p	GND	PEx16_0R(2)p	GND	PEx16_0R(0)p
	13	FPE_Bus_Err#	PEx16_x8_x4_0Clkn	PEx16_0R(7)p	PEx16_0R(6)n	PEx16_0R(5)p	PEx16_0R(4)n	PEx16_0R(3)p	PEx16_0R(2)n	PEx16_0R(1)p	PEx16_0R(0)n
	14	Config_Type0	GND	PEx16_0R(7)n	GND	PEx16_0R(5)n	GND	PEx16_0R(3)n	GND	PEx16_0R(1)n	GND
	15	Config_Type1	PEx16_x8_x4_1Clkp	GND	PEx16_0T(14)p	GND	PEx16_0T(12)p	GND	PEx16_0T(10)p	GND	PEx16_0T(8)p
	16	Config_Type2	PEx16_x8_x4_1Clkn	PEx16_0T(15)p	PEx16_0T(14)n	PEx16_0T(13)p	PEx16_0T(12)n	PEx16_0T(11)p	PEx16_0T(10)n	PEx16_0T(9)p	PEx16_0T(8)n
	17	Reserved	GND	PEx16_0T(15)n	GND	PEx16_0T(13)n	GND	PEx16_0T(11)n	GND	PEx16_0T(9)n	GND
	18	+12V	Reserved	GND	PEx16_0R(14)p	GND	PEx16_0R(12)p	GND	PEx16_0R(10)p	GND	PEx16_0R(8)p
	19	+12V	Reserved	PEx16_0R(15)p	PEx16_0R(14)n	PEx16_0R(13)p	PEx16_0R(12)n	PEx16_0R(11)p	PEx16_0R(10)n	PEx16_0R(9)p	PEx16_0R(8)n
	20	+12V	Reserved	PEx16_0R(15)n	GND	PEx16_0R(13)n	GND	PEx16_0R(11)n	GND	PEx16_0R(9)n	GND

C.2 FPE Profile-0 (User Defined)

Host: Config_Type(0:2) = 000 (“0” - Grounded)

Table 8-10: Connector B1 (FPE) Profile-0 Pin assignments

Top View Profile-0 Signals Assignment of Connector B1 (FPE)											
		ROWS									
		10	9	8	7	6	5	4	3	2	1
COLUMNS (EDGE OF THE BOARD)	1	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	AUX_CH+	HOT_PLUG
	2	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	AUX_CH-	GND
	3	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	DP_PWR	ML_L(1)p
	4	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	ML_L(3)p	ML_L(1)n
	5	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	ML_L(3)n	GND
	6	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	GND	ML_L(0)p
	7	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	User Defined	ML_L(2)p	ML_L(0)n
	8	User Defined	User Defined	User Defined	GND	User Defined	GND	User Defined	GND	ML_L(2)n	GND
	9	Reserved	Reserved	GND	PEx16_0T(6)p	GND	PEx16_0T(4)p	GND	PEx16_0T(2)p	GND	PEx16_0T(0)p
	10	Reserved	Reserved	PEx16_0T(7)p	PEx16_0T(6)n	PEx16_0T(5)p	PEx16_0T(4)n	PEx16_0T(3)p	PEx16_0T(2)n	PEx16_0T(1)p	PEx16_0T(0)n
	11	PE_RST#	GND	PEx16_0T(7)n	GND	PEx16_0T(5)n	GND	PEx16_0T(3)n	GND	PEx16_0T(1)n	GND
	12	GND	PEx16_x8_x4_0Clkp	GND	PEx16_0R(6)p	GND	PEx16_0R(4)p	GND	PEx16_0R(2)p	GND	PEx16_0R(0)p
	13	FPE_Bus_Err#	PEx16_x8_x4_0Clkn	PEx16_0R(7)p	PEx16_0R(6)n	PEx16_0R(5)p	PEx16_0R(4)n	PEx16_0R(3)p	PEx16_0R(2)n	PEx16_0R(1)p	PEx16_0R(0)n
	14	Config_Type0	GND	PEx16_0R(7)n	GND	PEx16_0R(5)n	GND	PEx16_0R(3)n	GND	PEx16_0R(1)n	GND
	15	Config_Type1	PEx16_x8_x4_1Clkp	GND	PEx16_0T(14)p	GND	PEx16_0T(12)p	GND	PEx16_0T(10)p	GND	PEx16_0T(8)p
	16	Config_Type2	PEx16_x8_x4_1Clkn	PEx16_0T(15)p	PEx16_0T(14)n	PEx16_0T(13)p	PEx16_0T(12)n	PEx16_0T(11)p	PEx16_0T(10)n	PEx16_0T(9)p	PEx16_0T(8)n
	17	Reserved	GND	PEx16_0T(15)n	GND	PEx16_0T(13)n	GND	PEx16_0T(11)n	GND	PEx16_0T(9)n	GND
	18	+12V	Reserved	GND	PEx16_0R(14)p	GND	PEx16_0R(12)p	GND	PEx16_0R(10)p	GND	PEx16_0R(8)p
	19	+12V	Reserved	PEx16_0R(15)p	PEx16_0R(14)n	PEx16_0R(13)p	PEx16_0R(12)n	PEx16_0R(11)p	PEx16_0R(10)n	PEx16_0R(9)p	PEx16_0R(8)n
	20	+12V	Reserved	PEx16_0R(15)n	GND	PEx16_0R(13)n	GND	PEx16_0R(11)n	GND	PEx16_0R(9)n	GND

This Profile indicates that Configurable Section is User Defined. For this Profile vendor is free to implement any application specific requirements using Configurable Section pins. It can be used for example for special communication link between DSP peripheral modules, for cable free connection to external interfaces, for customizing CPU module for special COM applications, etc.

C.3 FPE Profile-1 (USB 3.0)

Host: Config_Type(0:2) = 100

Config_Type0= 1 (10K Pull-up)

Config_Type(1:2)= 00 (Grounded)

Table 8-11: Connector B1 (FPE) Profile-1 Pin assignments

Top View Profile-1 Signals Assignment of Connector B1 (FPE)											
		ROWS									
		10	9	8	7	6	5	4	3	2	1
COLUMNS (EDGE OF THE BOARD)	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AUX_CH+	HOT_PLUG
	2	Reserved	Reserved	Reserved	GND	Reserved	GND	Reserved	GND	AUX_CH-	GND
	3	Reserved	Reserved	GND	USB3_2SS TXp	GND	USB3_1SS TXp	GND	USB3_0SS TXp	DP_PWR	ML_L(1)p
	4	Reserved	Reserved	USB3_2SS RXp	USB3_2SS TXn	USB3_1SS RXp	USB3_1SS TXn	USB3_0SS RXp	USB3_0SS TXn	ML_L(3)p	ML_L(1)n
	5	Reserved	GND	USB3_2SS RXn	GND	USB3_1SS RXn	GND	USB3_0SS RXn	GND	ML_L(3)n	GND
	6	Reserved	Reserved	GND	USB3_3SS TXp	GND	USB3_4SS TXp	GND	USB3_5SS TXp	GND	ML_L(0)p
	7	Reserved	Reserved	USB3_3SS RXp	USB3_3SS TXn	USB3_4SS RXp	USB3_4SS TXn	USB3_5SS RXp	USB3_5SS TXn	ML_L(2)p	ML_L(0)n
	8	Reserved	GND	USB3_3SS RXn	GND	USB3_4SS RXn	GND	USB3_5SS RXn	GND	ML_L(2)n	GND
	9	Reserved	Reserved	GND	PEx16_0T(6)p	GND	PEx16_0T(4)p	GND	PEx16_0T(2)p	GND	PEx16_0T(0)p
	10	Reserved	Reserved	PEx16_0T(7)p	PEx16_0T(6)n	PEx16_0T(5)p	PEx16_0T(4)n	PEx16_0T(3)p	PEx16_0T(2)n	PEx16_0T(1)p	PEx16_0T(0)n
	11	PE_RST#	GND	PEx16_0T(7)n	GND	PEx16_0T(5)n	GND	PEx16_0T(3)n	GND	PEx16_0T(1)n	GND
	12	GND	PEx16_x8_x4_0Clkp	GND	PEx16_0R(6)p	GND	PEx16_0R(4)p	GND	PEx16_0R(2)p	GND	PEx16_0R(0)p
	13	FPE_Bus_Err#	PEx16_x8_x4_0Clkn	PEx16_0R(7)p	PEx16_0R(6)n	PEx16_0R(5)p	PEx16_0R(4)n	PEx16_0R(3)p	PEx16_0R(2)n	PEx16_0R(1)p	PEx16_0R(0)n
	14	Config_Type0	GND	PEx16_0R(7)n	GND	PEx16_0R(5)n	GND	PEx16_0R(3)n	GND	PEx16_0R(1)n	GND
	15	Config_Type1	PEx16_x8_x4_1Clkp	GND	PEx16_0T(14)p	GND	PEx16_0T(12)p	GND	PEx16_0T(10)p	GND	PEx16_0T(8)p
	16	Config_Type2	PEx16_x8_x4_1Clkn	PEx16_0T(15)p	PEx16_0T(14)n	PEx16_0T(13)p	PEx16_0T(12)n	PEx16_0T(11)p	PEx16_0T(10)n	PEx16_0T(9)p	PEx16_0T(8)n
	17	Reserved	GND	PEx16_0T(15)n	GND	PEx16_0T(13)n	GND	PEx16_0T(11)n	GND	PEx16_0T(9)n	GND
	18	+12V	Reserved	GND	PEx16_0R(14)p	GND	PEx16_0R(12)p	GND	PEx16_0R(10)p	GND	PEx16_0R(8)p
	19	+12V	Reserved	PEx16_0R(15)p	PEx16_0R(14)n	PEx16_0R(13)p	PEx16_0R(12)n	PEx16_0R(11)p	PEx16_0R(10)n	PEx16_0R(9)p	PEx16_0R(8)n
	20	+12V	Reserved	PEx16_0R(15)n	GND	PEx16_0R(13)n	GND	PEx16_0R(11)n	GND	PEx16_0R(9)n	GND

This Configurable Section Profile defines 6 USB 3.0 SuperSpeed ports. These ports should be used together with 6 USB 2.0 ports defined for StackPC Expansion Connector A. Link Shifting is applicable.

APPENDIX D: StackPC and StackPWR Layout & Dimensions (Adoption to PC/104 standard form-factor)

If StackPC approach adapting to PC/104 form-factor, then all mechanical requirements of PC/104 should be met. StackPC expansion connector has the same type and layout as PCIe/104.

Locations of StackPWR-1, 2, 3 connectors are the same for StackPC, StackPC-PCI and StackPC-FPE HOST and Power Source modules.

Detailed StackPC connectors mutual layout is shown on Figure 8-11: StackPC Layout & Dimensions.

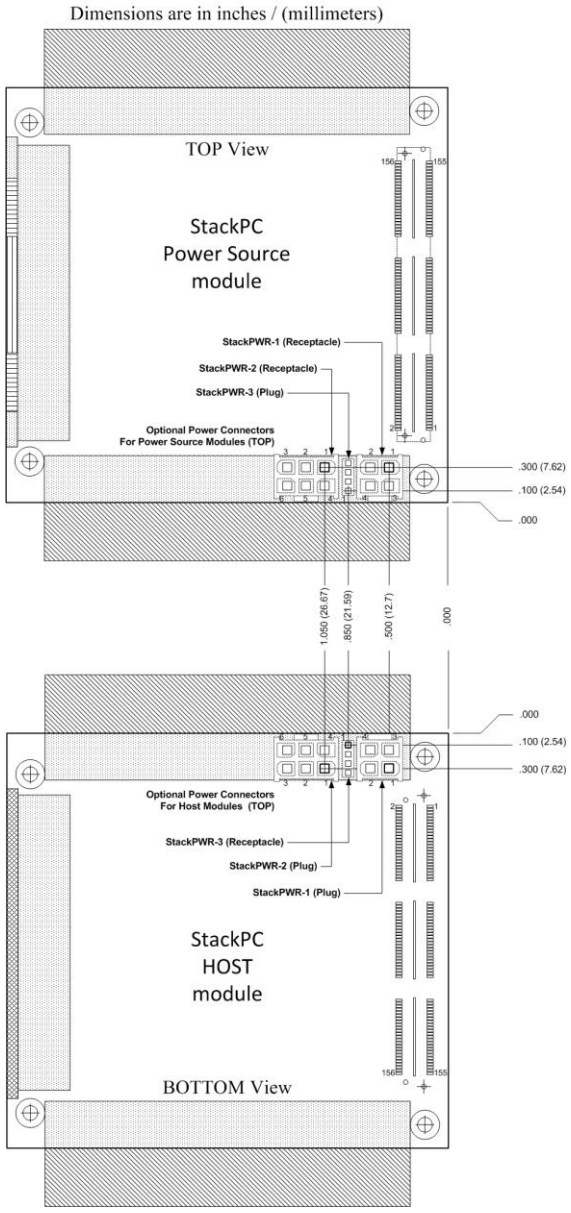


Figure 8-28: StackPWR connectors location for StackPC module (PC/104 adopted)

APPENDIX E: StackPC-PCI Layout & Dimensions (Adoption to PC/104 standard form-factor)

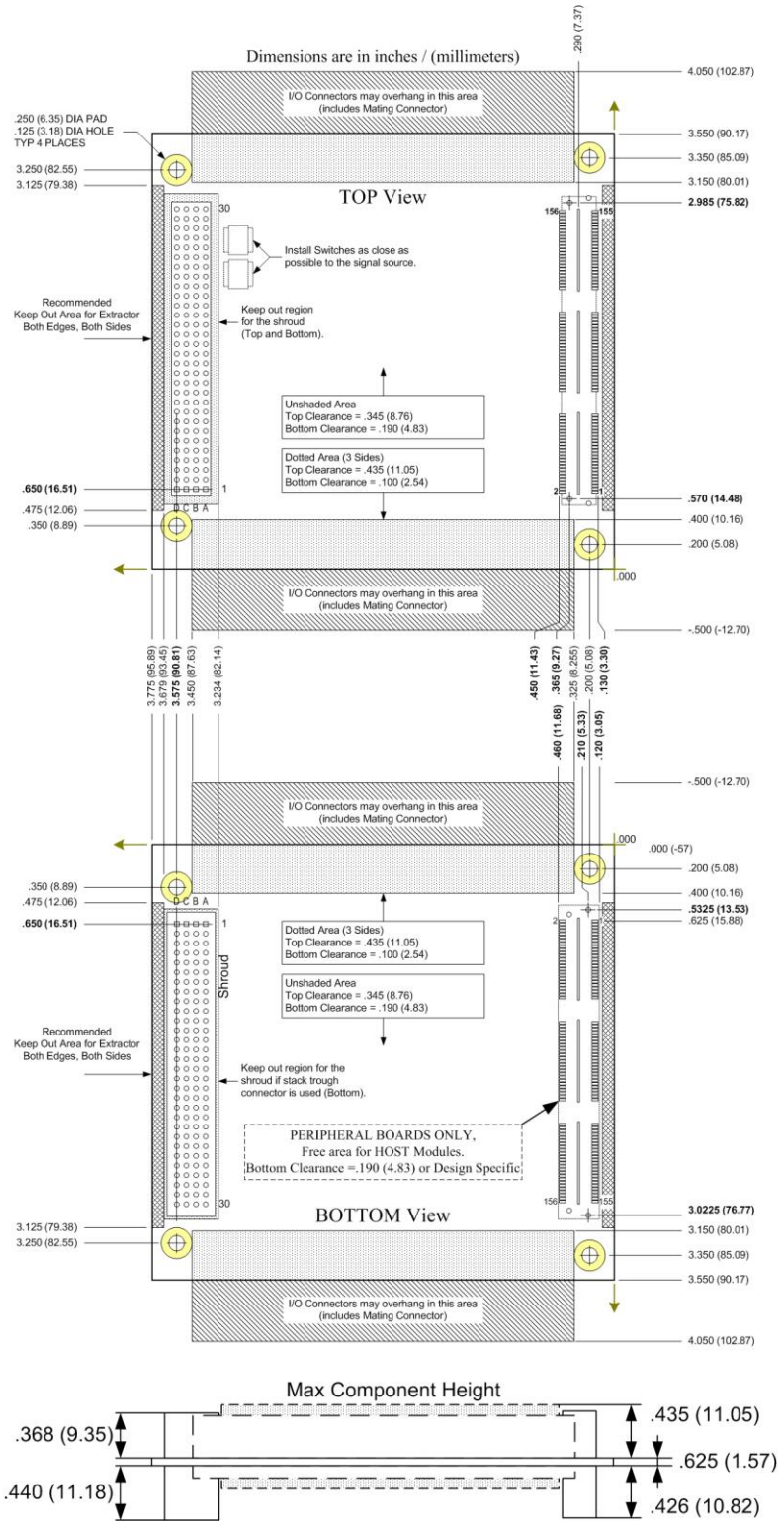


Figure 8-29: StackPC-PCI Module Dimensions (PC/104 adopted)

APPENDIX F: StackPC-FPE Layout & Dimensions (Adoption to PC/104 standard form-factor)

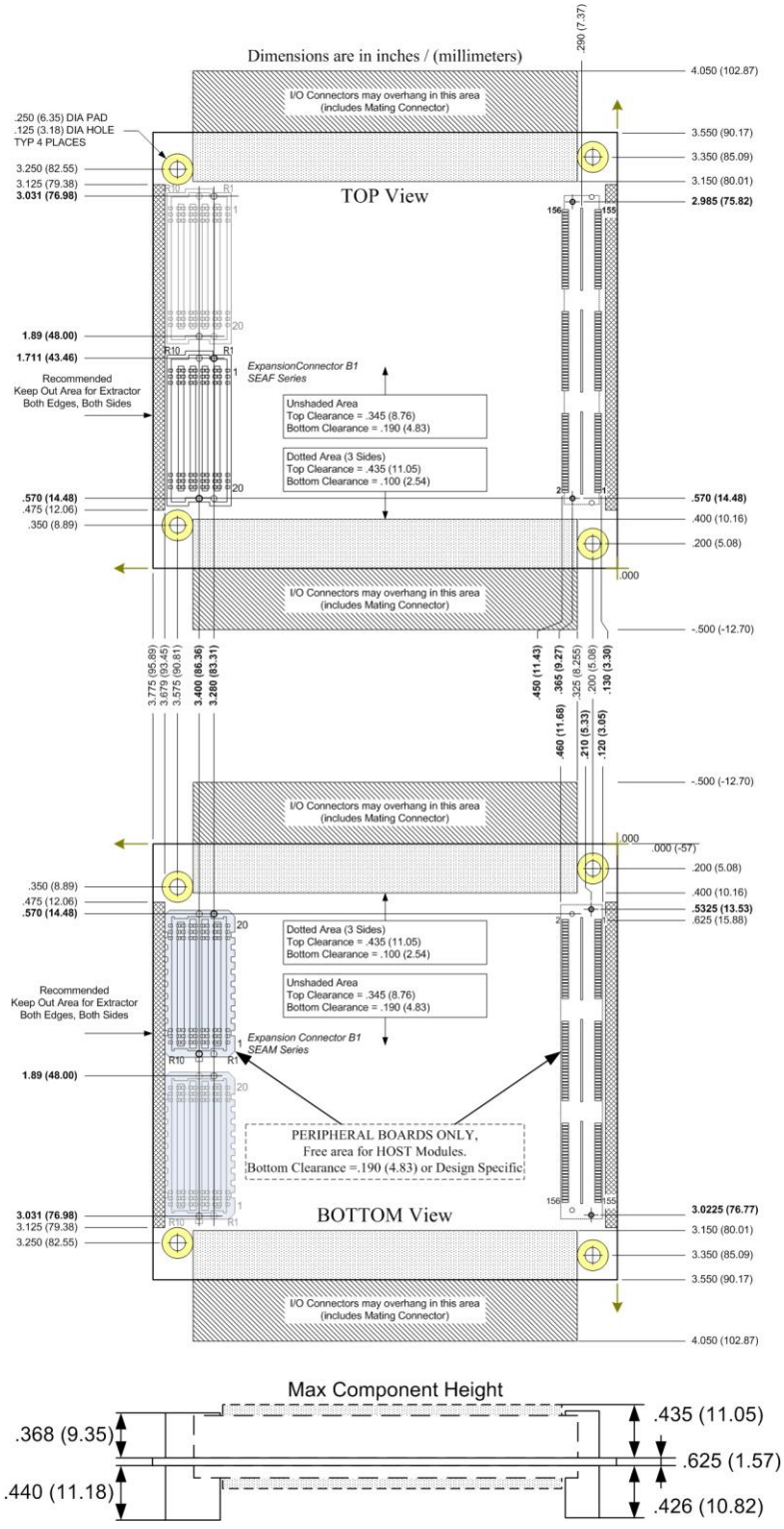


Figure 8-30: StackPC-FPE Module Dimensions (PC/104 adopted)

APPENDIX G: EPIC SBC with StackPC support (Adoption to EPIC standard form-factor)

Single Board Computer of EPIC form-factor can be easily created with support of StackPC Expansion Connectors on TOP side.

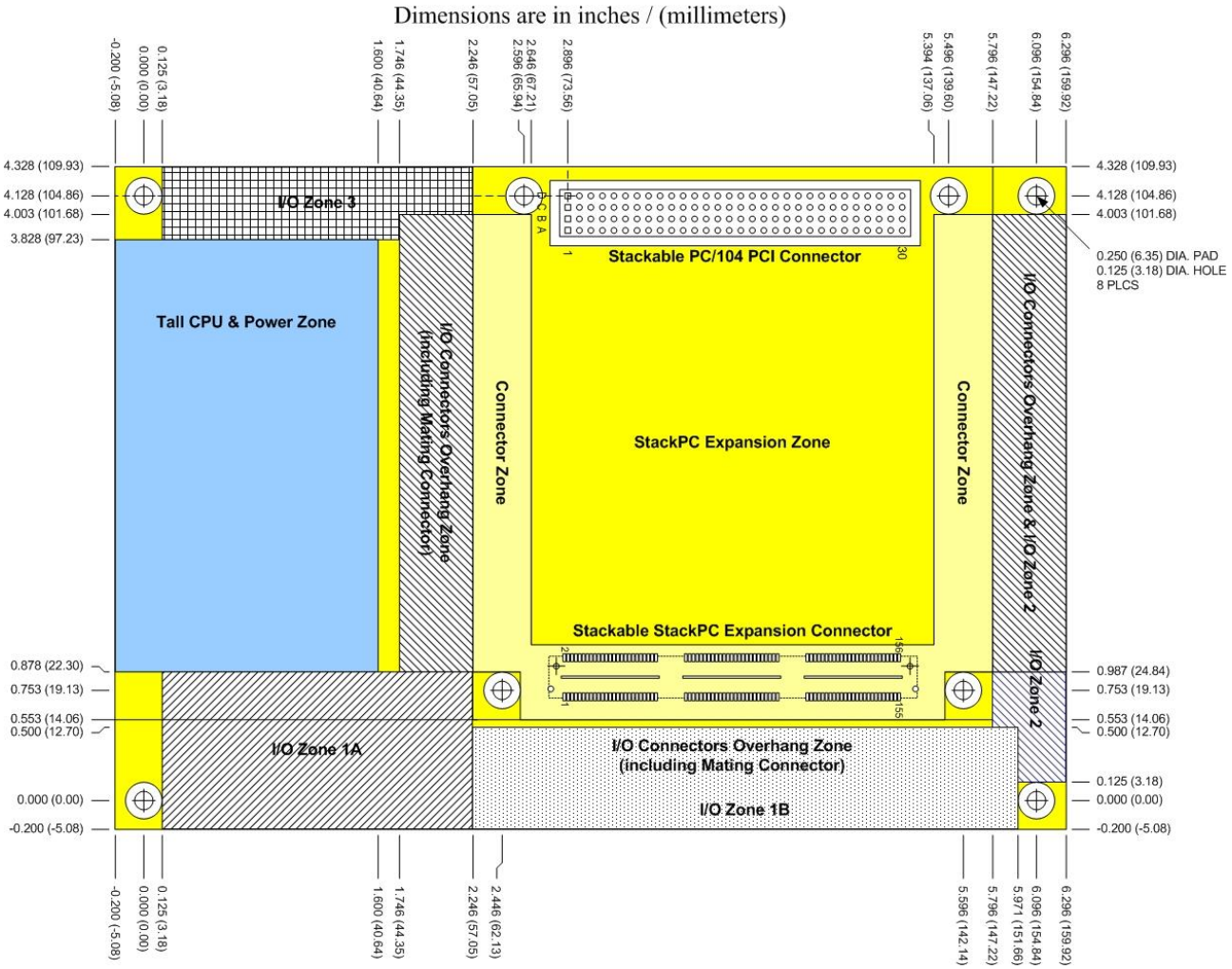


Figure 8-31: EPIC with StackPC-PCI (EPIC adopted)

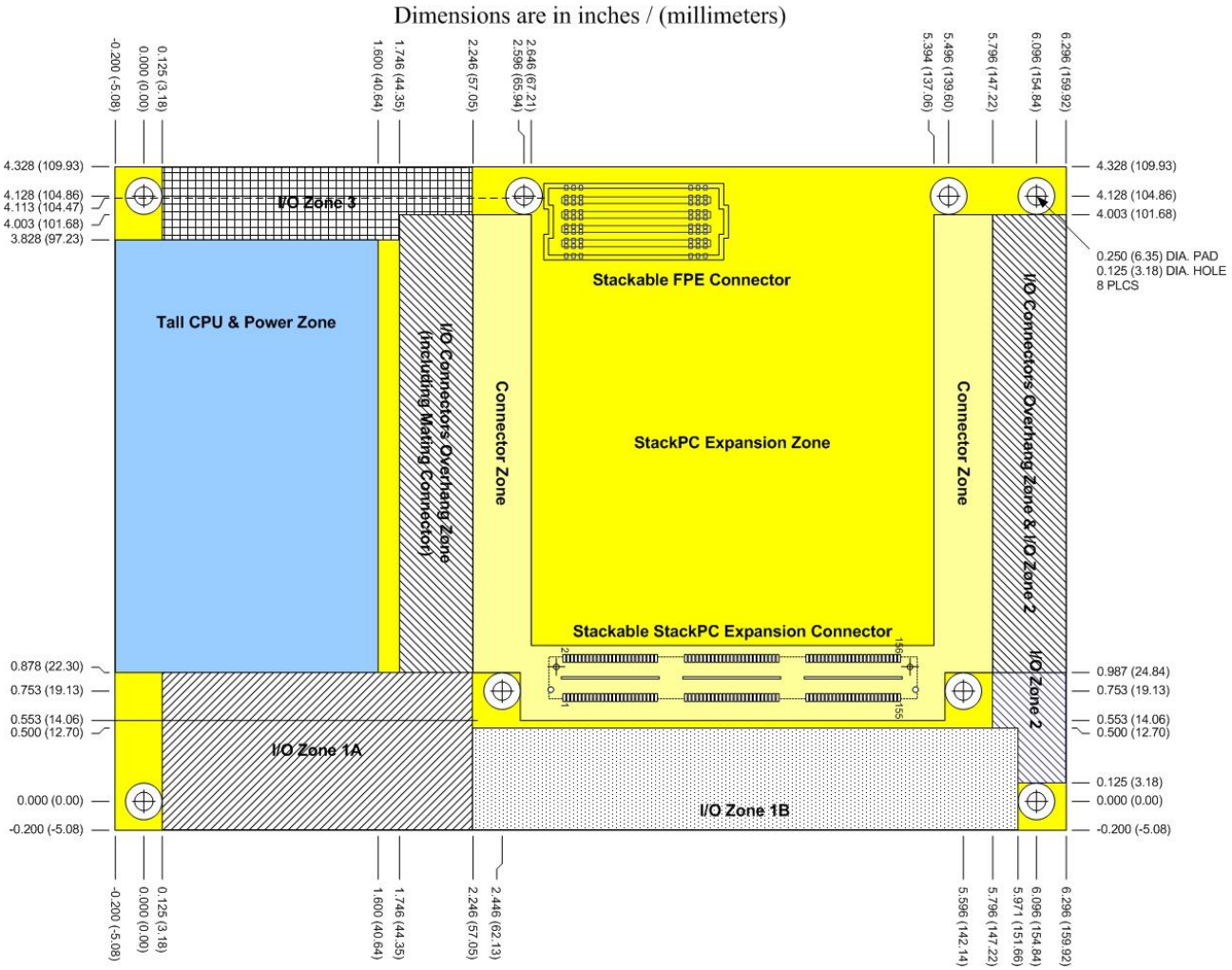


Figure 8-32: EPIC with StackPC-FPE (EPIC adopted)

APPENDIX H: EBX SBC with StackPC support (Adoption to EBX standard form-factor)

Single Board Computer of EBX form-factor can be easily created with support of StackPC Expansion Connectors on TOP side.

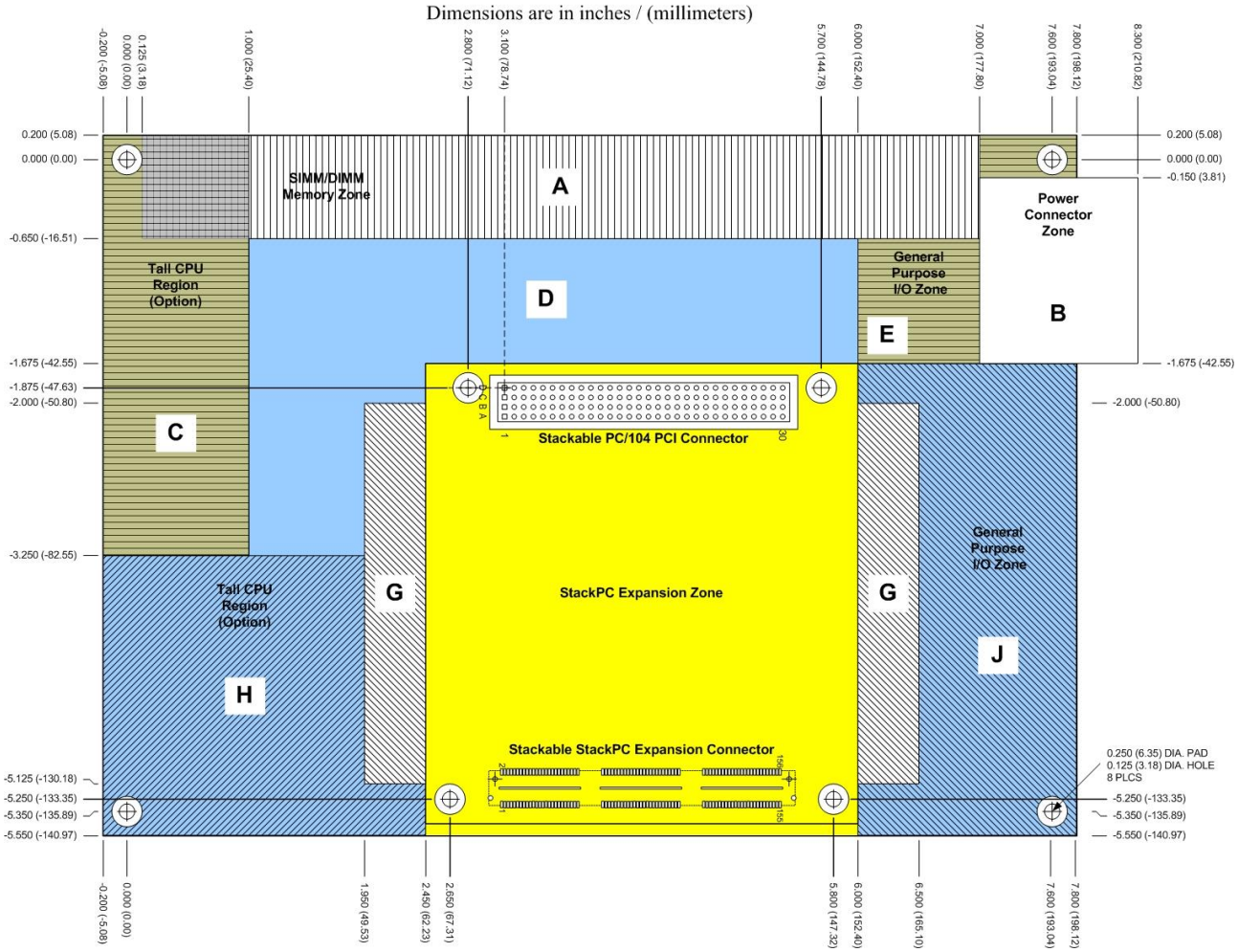


Figure 8-33: EBX with StackPC-PCI (EBX adopted)

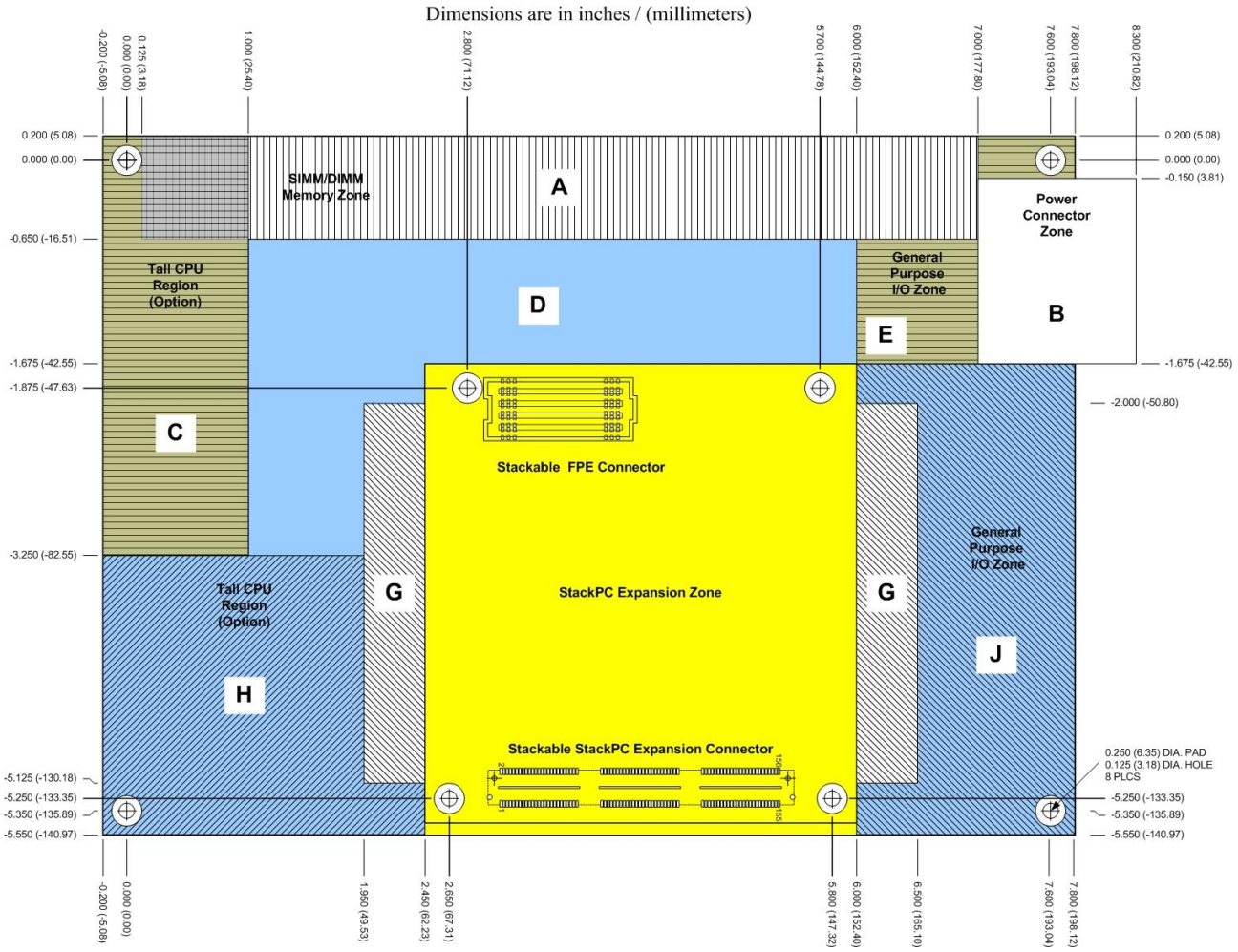


Figure 8-34: EBX with StackPC-FPE (EBX adopted)

APPENDIX I: 3.5” SBC with StackPC support (Adoption to 3,5” standard form-factor)

Single Board Computer of 3,5” form-factor can be easily created with support of StackPC Expansion Connectors on TOP side.

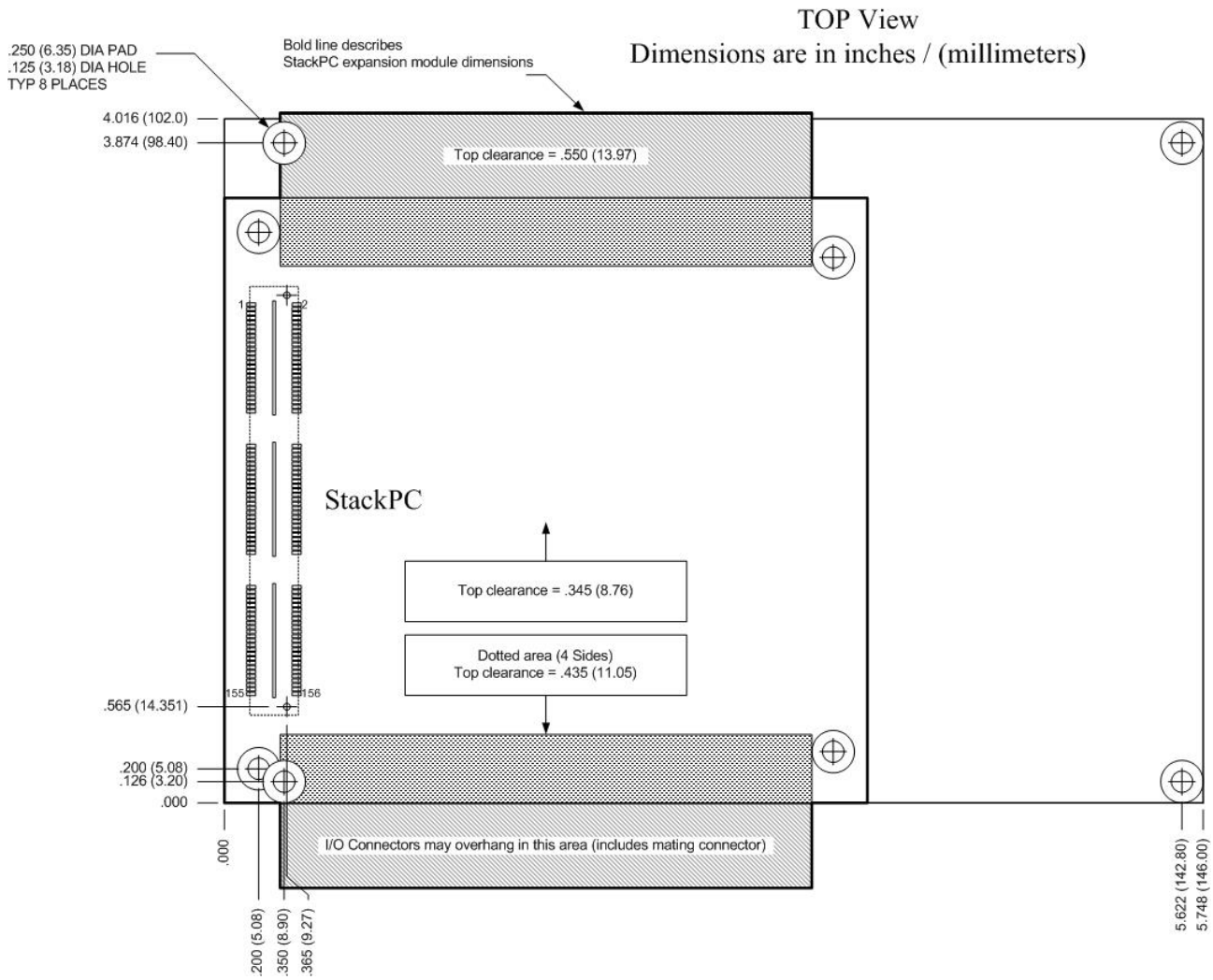


Figure 8-35: 3.5” with StackPC (3,5” adopted)

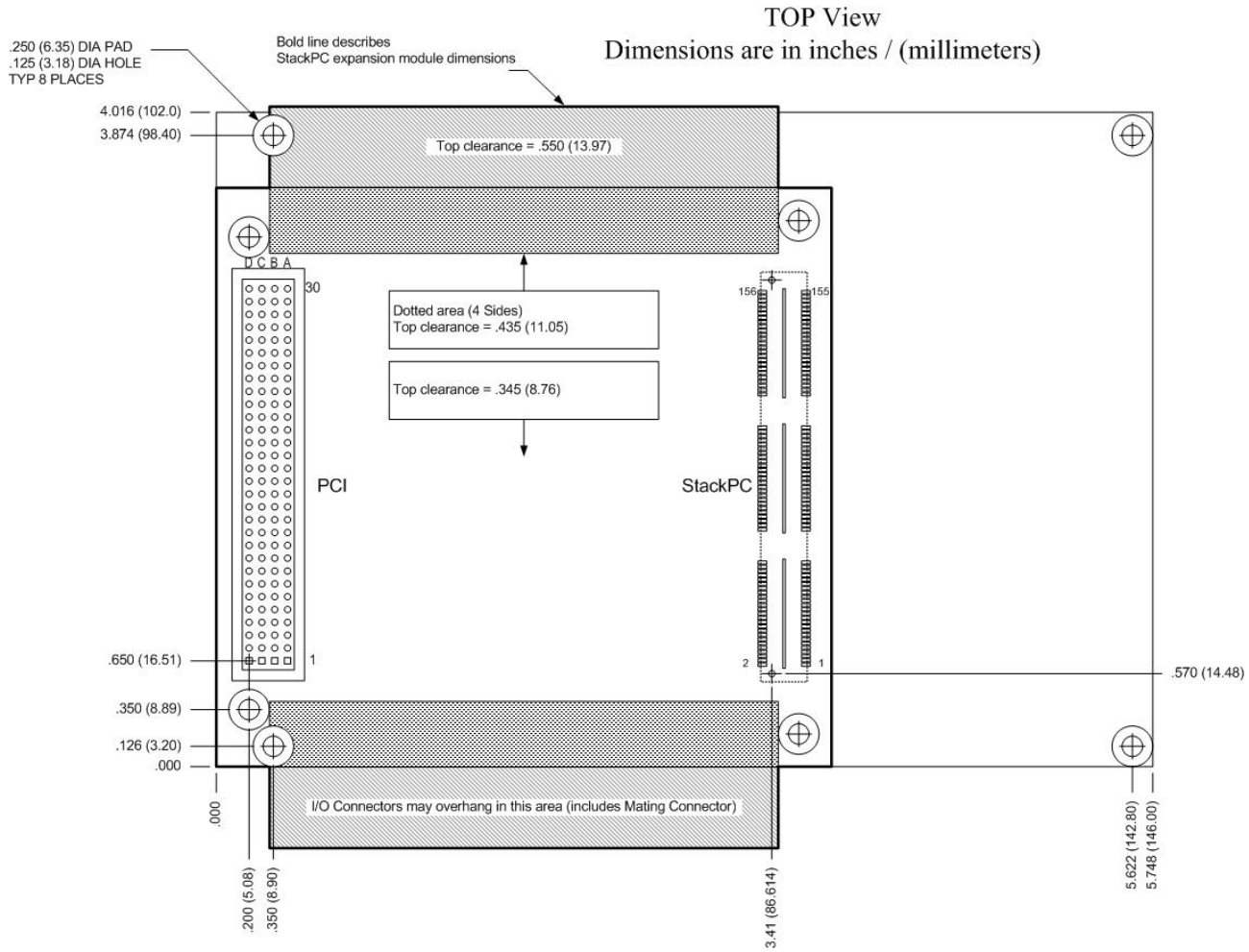


Figure 8-36: 3.5” with StackPC-PCI (3,5” adopted)

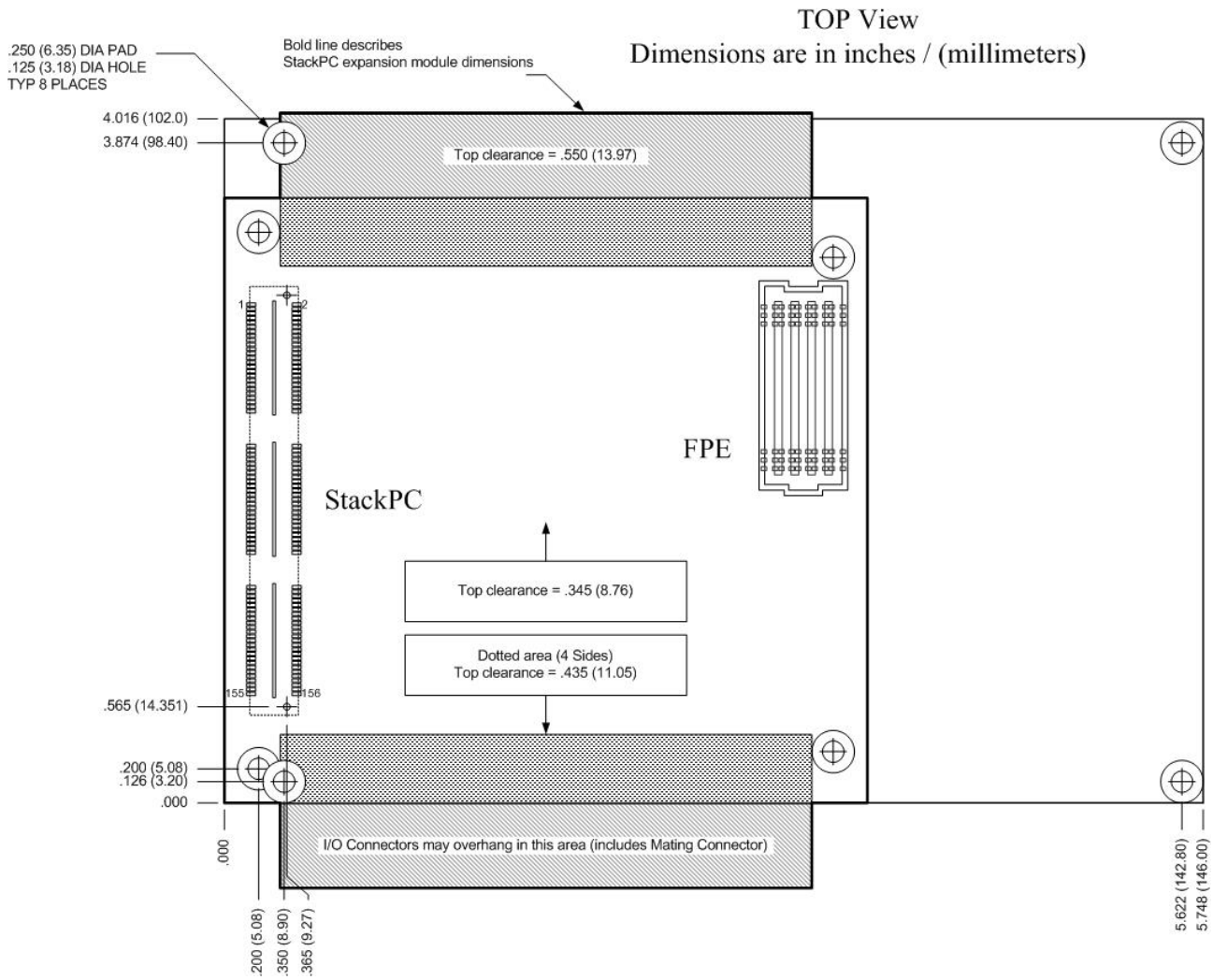


Figure 8-37: 3.5” with StackPC-FPE (3,5” adopted)